EE 435

Lecture 24

Noise in Operational Amplifiers

Common-Mode Feedback

Output Stages

Where we are at on amplifier topic:

Operation
Synthesis
Architectures
Compensation
Design Principle

- Linearity
- Offset voltage : Gradient Effects
- Layout of Analog Circuits (brief)
- Noise in Operational Amplifiers
- Output Stages
- Common-mode feedback

} Monday

Review from last lecture

Common Centroid Layouts

Almost Theorem:

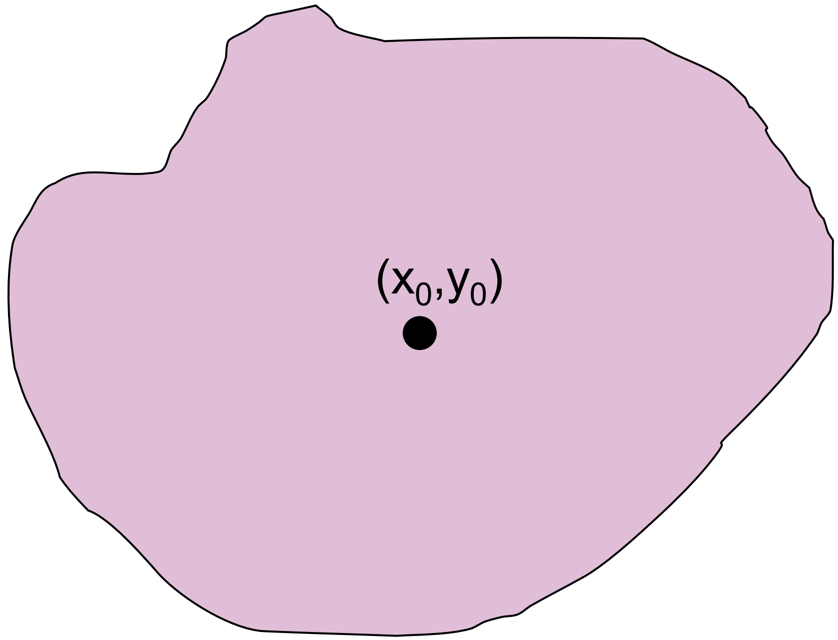
If p(x,y) varies linearly throughout a two-dimensional region, then $p_{EQ}=p(x_0.y_0)$ where x_0,y_0 is the geometric centroid to the region.

If a parameter varies linearly throughout a two-dimensional region, it is said to have a linear gradient.

Many parameters have a dominantly linear gradient over rather small regions but large enough to encompass layouts where devices are ideally matched

Review from last lecture

Common Centroid Layouts



(x_0,y_0) is geometric centroid

$$\mathbf{p_{EQ} = \frac{1}{A}\int_A p(x,y)\,dx\,dy}$$

If ρ(x,y) varies linearly in any direction, then the theorem states

$$p_{EQ} = \frac{1}{A}\int_A p(x,y)\,dx\,dy = p(x_0,y_0)$$

Common Centroid Layouts

Definition: A layout of two devices is termed a common-centroid layout if both devices have the same geometric centroid

Almost Theorem:

If p(x,y) varies linearly throughout a two-dimensional region, then if two devices have the same centroid, the linear-variable parameters are matched !

Note: This is true independent of the magnitude and direction of the gradient!

Almost Theorem:

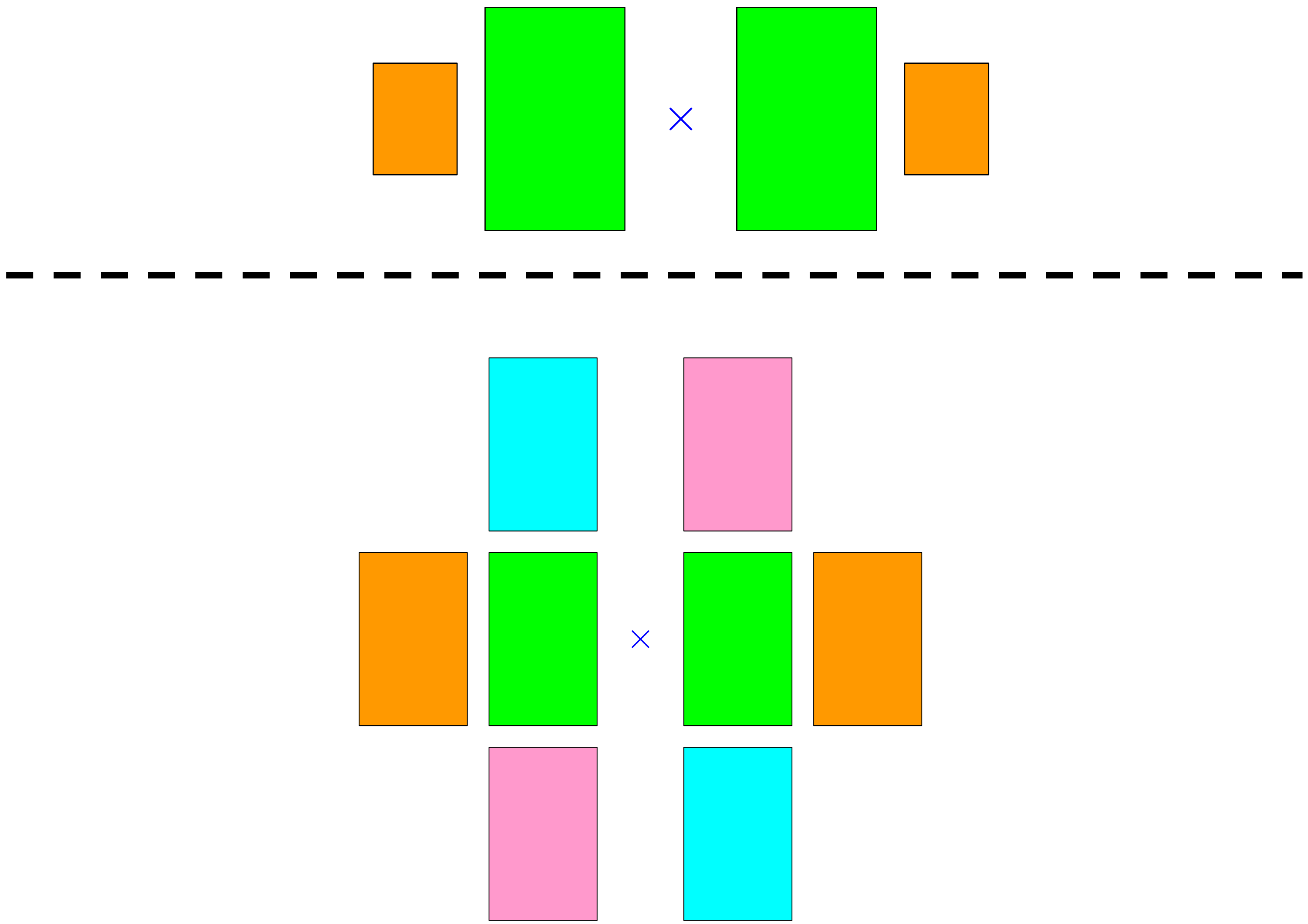
If a common-centroid layout is used for the matching-critical part of an operational amplifier, the linear part of the linear-variable parameters (e.g. V_{TH}, μ, C_{OX}) will introduce no offset voltage!

Common-centroid layouts almost always used for matching-critical components to eliminate linear gradients of critical parameters !

But local random variations will still affect matching even if gradient effects are eliminated

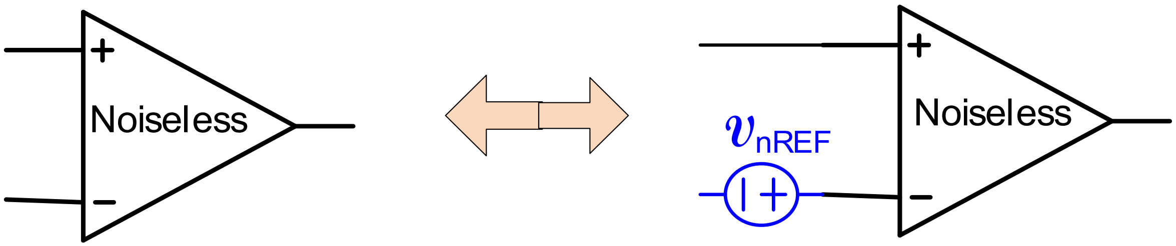
Review from last lecture

Common Centroid of Multiple Segmented Geometries



Review from last lecture

Noise in Operational Amplifiers



All noise sources in an op amp can be referred to a single noise source

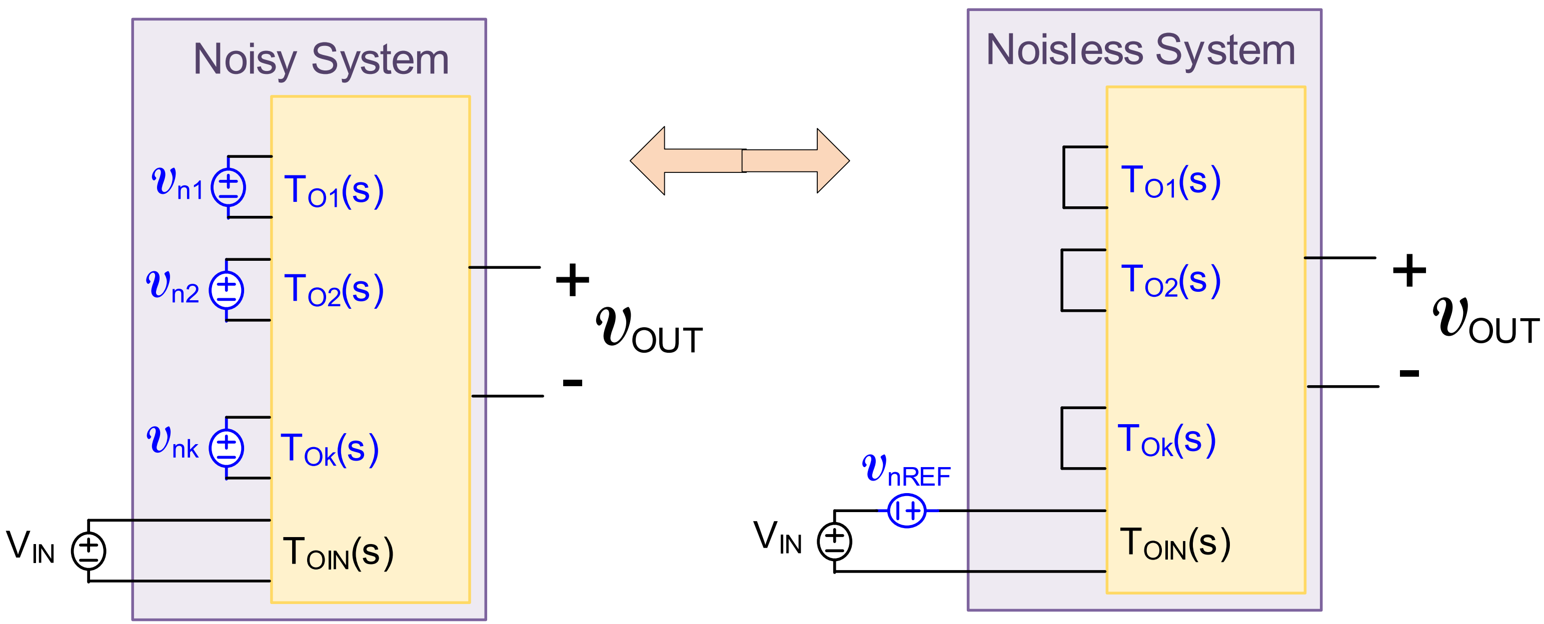
Noise can be referred to either input terminal

Characterized by spectral density S

Can add offset voltage as well

Review from last lecture

Noise Analysis Review



If all noise sources are uncorrelated (the usual situation for device noise sources)

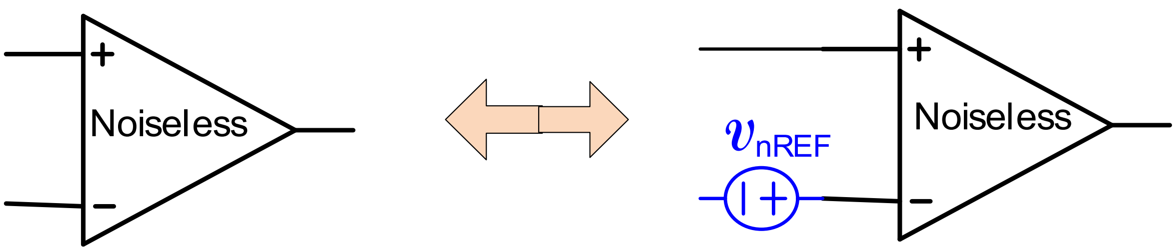
$$S_{OUT} = \sum_{i=1}^{k} S_k \left|T_{Oi}(j\omega)\right|^2$$

$$V_{O\_RMS} = \sqrt{\int_{f=0}^{\infty} S_{OUT}\,\mathbf{df}}$$

$$S_{IN} = \frac{S_{IN}}{\left|T_{OIN}(j\omega)\right|^2} = \frac{\sum_{i=1}^{k} S_k \left|T_{Oi}(j\omega)\right|^2}{\left|T_{OIN}(j\omega)\right|^2}$$

Review from last lecture

Noise in Operational Amplifiers

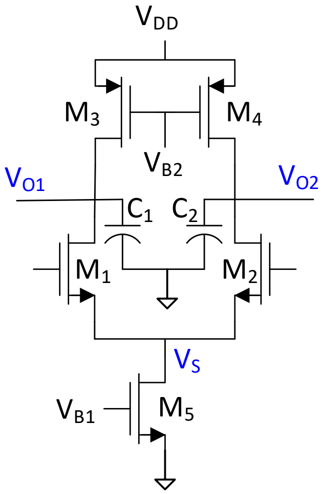


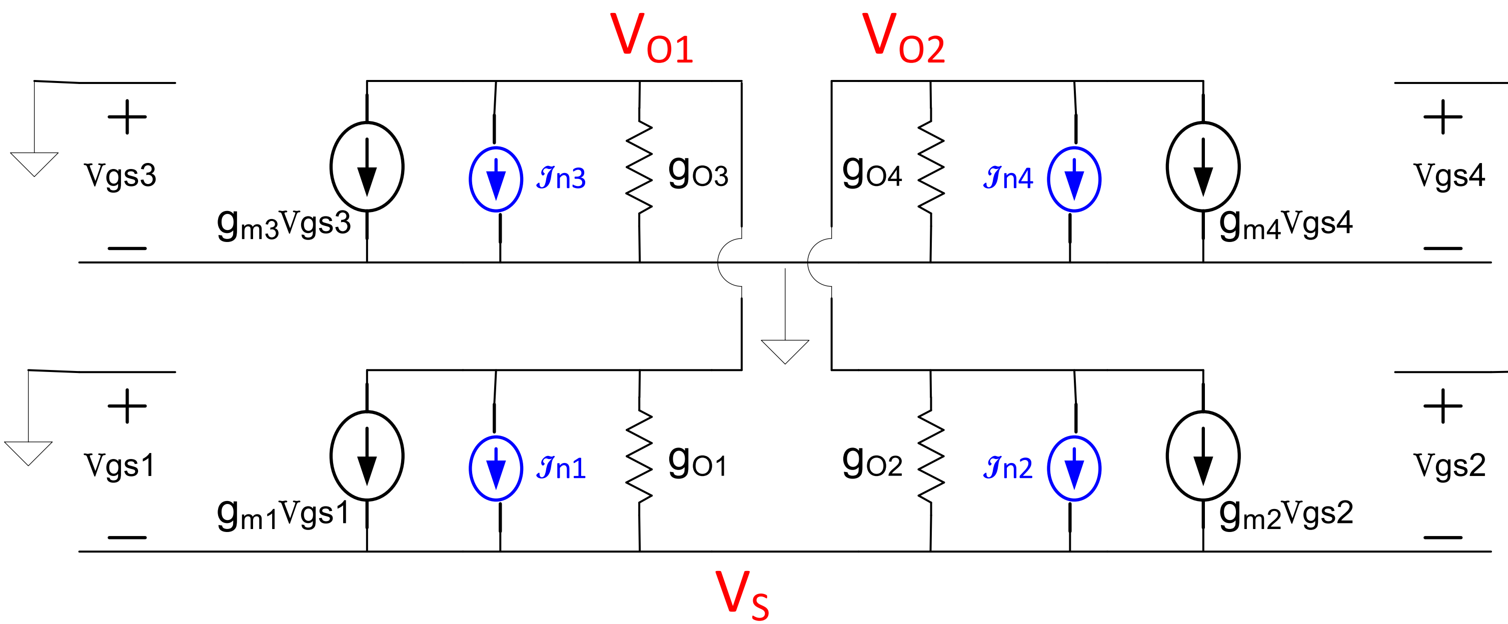
Noise in an op amp almost entirely dominated by noise in input stage

Usually suffices to study noise of only input stage

Review from last lecture

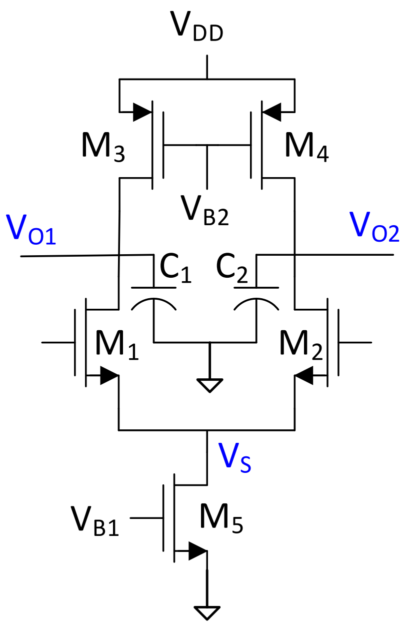
Consider 5T Op Amp (Current Source Bias)

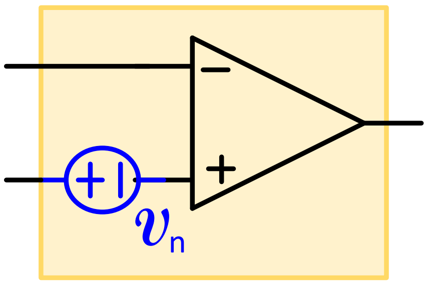




$$S_k = \frac{8kT}{3} g_{mk}$$

Consider 5T Op Amp (Current Source Bias)



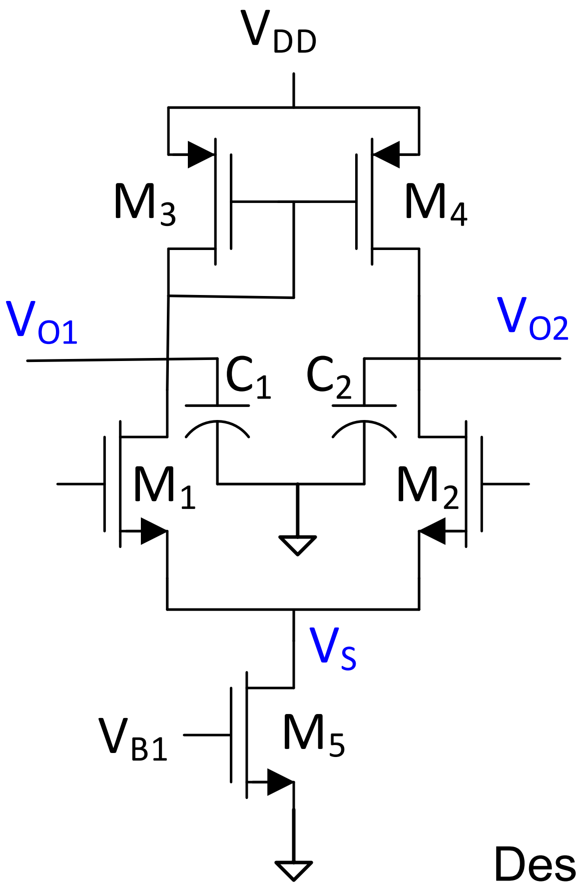


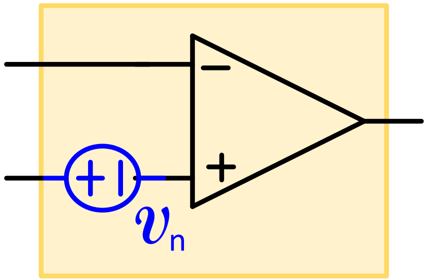
$$S_{IN} = \frac{16kT\mathrm{V}_{\mathrm{DD}}}{3\mathrm{P}} \bullet \mathrm{V}_{\mathrm{EB1}}\left(1+5\frac{V_{EB1}}{V_{EB3}}\right)$$

Designer has considerable control with V_{EB1} and V_{EB3}

But key parameter is P with reducing V_{RMS} by factor of 10 requiring a factor of 100 increase in power!

Consider 5T Op Amp (Mirror Bias)





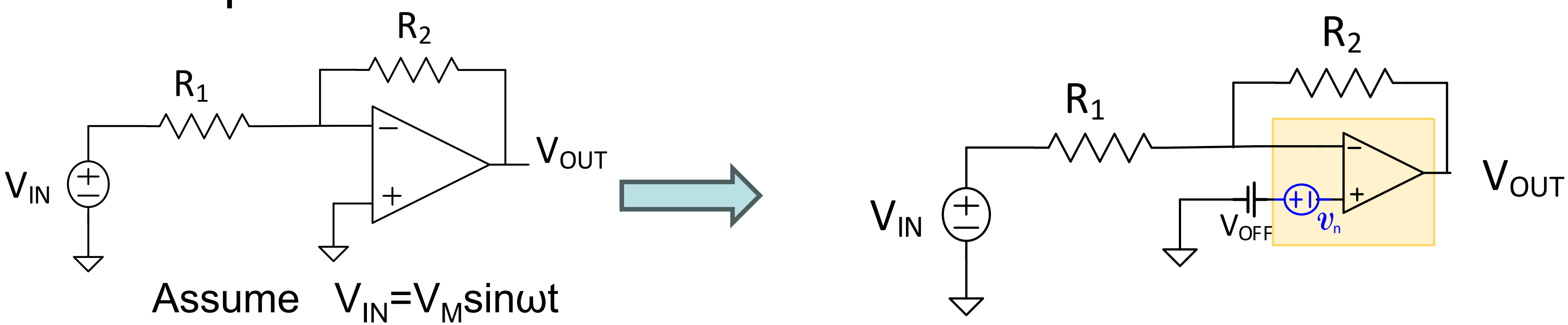
$$S_{VIN} = \frac{16kTV_{DD}}{3P} \bullet V_{EB1}\left(1+\frac{V_{EB1}}{V_{EB3}}\right)$$

Designer has considerable control with V_{EB1} and V_{EB3}

But key parameter is P with reducing V_{RMS} by factor of 10 requiring a factor of 100 increase in power!

Review from last lecture

Example:



Assume $V_{IN}=V_M\sin\omega t$

Noise Output:

$$A(s)=\frac{A_0 p}{s+p}$$

$$p=\frac{GB}{A_0}$$

$$V_{ON}=\frac{A(s)}{1+\beta A(s)}v_n=A_{FB}(s)v_n$$

$$S_{OUT}=S_{IN}\left|A_{FB}(j\omega)\right|^2$$

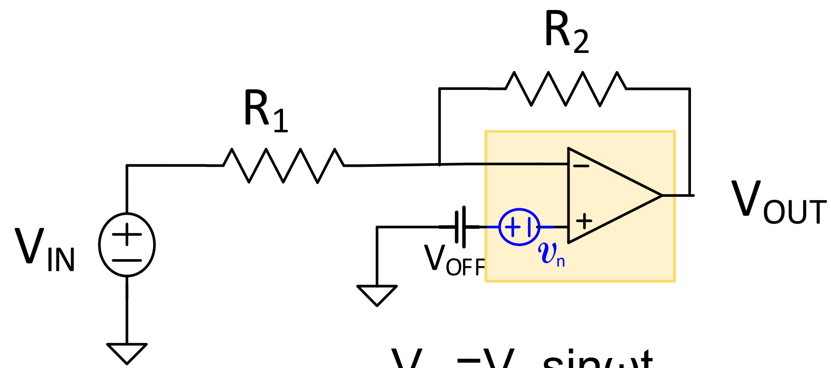
$$V_{nRMS\_Out}=\sqrt{\int_{f=0}^{\infty}S_{IN}\left|A_{FB}(j\omega)\right|^2 df}$$

$$V_{SIG\_RMS\_Out}=\frac{V_M}{\sqrt{2}}\left(1+\frac{R_2}{R_1}\right)$$

$$SNR=\frac{\frac{V_M}{\sqrt{2}}\left(1+\frac{R_2}{R_1}\right)}{\sqrt{\int_{f=0}^{\infty}S_{IN}\left|A_{FB}(j\omega)\right|^2 df}}$$

SNR Calculation in Example Circuit

$$SNR=\frac{\frac{V_M}{\sqrt{2}}\left(1+\frac{R_2}{R_1}\right)}{\sqrt{\int_{f=0}^{\infty} S_{IN}\left|A_{FB}(j\omega)\right|^2 df}}$$



$V_{IN}=V_M \sin\omega t$

$$S_{vn}=\frac{16kTV_{DD}}{3P}\bullet V_{EB1}\left(1+\frac{V_{EB1}}{V_{EB3}}\right)$$

$$A(s)=\frac{A_0 p}{s+p}=\frac{GB}{s+p}\simeq\frac{GB}{s}$$

$$A_{FB}(s)=\frac{-\frac{R_2}{R_1}}{1+\frac{s}{GB}\left(1+\frac{R_2}{R_1}\right)}$$

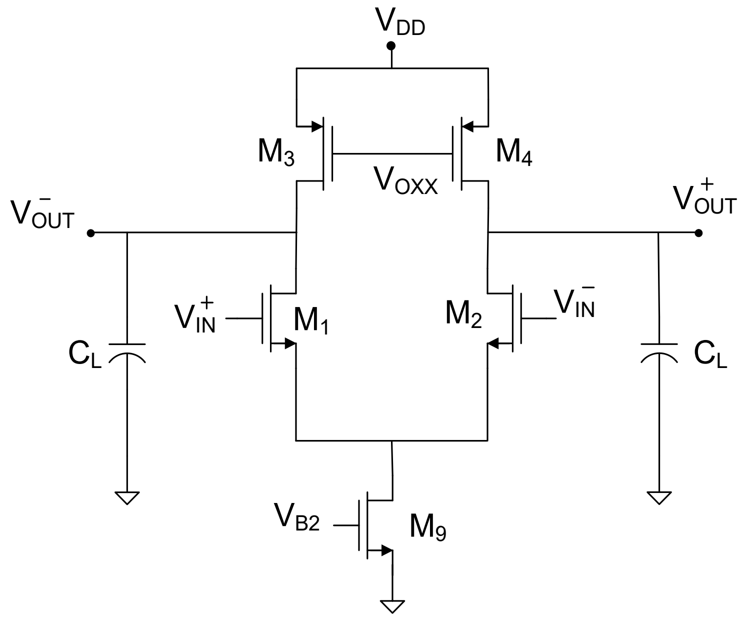
$$\left|A_{FB}(j\omega)\right|^2=\frac{\left(\frac{R_2}{R_1}\right)^2}{1+\omega^2\left(\left(1+\frac{R_2}{R_1}\right)\frac{1}{GB}\right)^2}=\left(\frac{R_2}{R_1+R_2}GB\right)^2\bullet\frac{1}{\left(GB\frac{R_1}{R_1+R_2}\right)^2+\omega^2}$$

Useful trig identity for calculating SNR

$$\int_{f=0}^{\infty}\frac{1}{b^2+\omega^2}df=\frac{1}{4b}$$

Can now substitute back into expression for SNR for closed-form analytical solution

Common-Mode Feedback

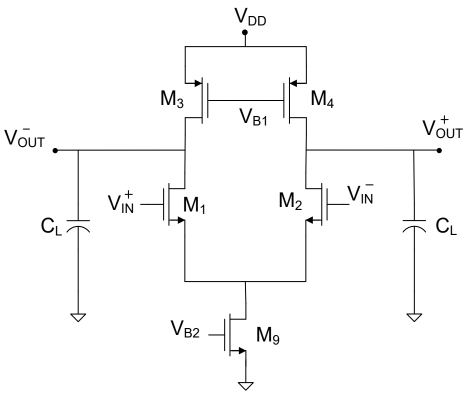


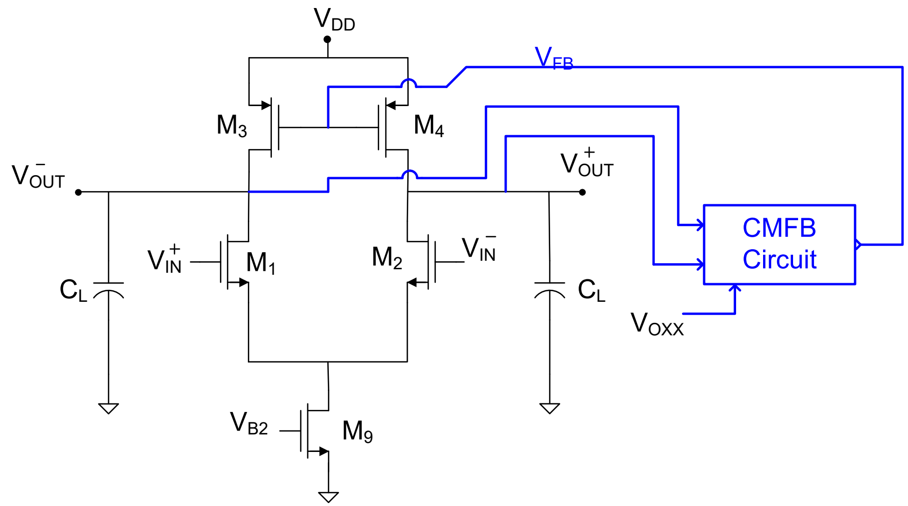
Needs CMFB

Repeatedly throughout the course, we have added a footnote on fully-differential circuits that a common-mode feedback circuit (CMFB) is needed for some circuits

If required, the CMFB circuit establishes or “stabilizes” the operating point or operating points of the op amp

Common-Mode Feedback





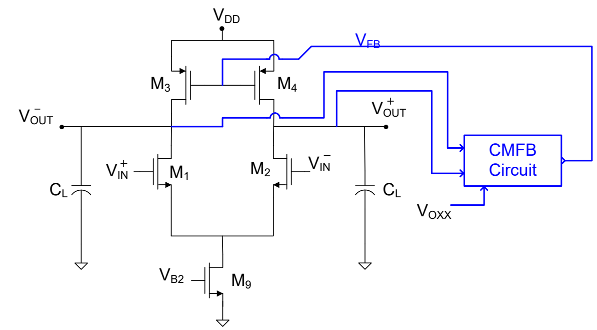
On the reference op amp, the CMFB signal can be applied to either the p-channel biasing transistors or to the tail current transistor

It is usually applied only to a small portion of the biasing transistors though often depicted as shown

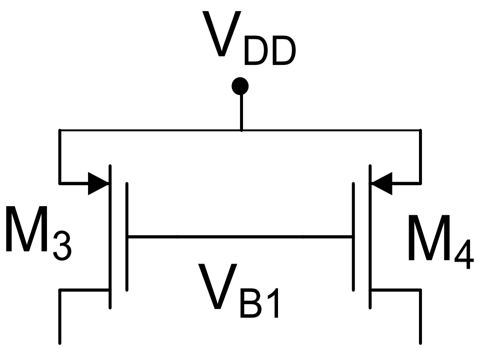
There is often considerable effort devoted to the design of the CMFB though little details are provided in most books and the basic concepts of the CMFB are seldom rigorously developed and often misunderstood

Common-Mode Feedback

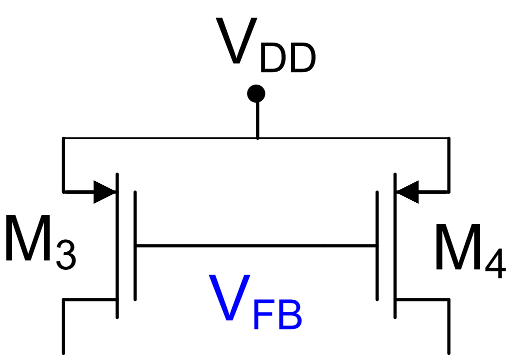
Partitioning biasing transistors for V_{FB} insertion



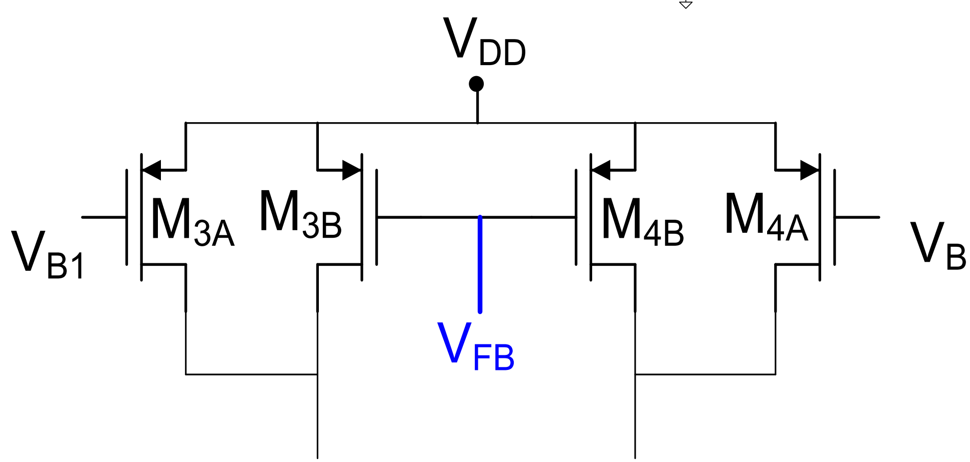
(Nominal device matching assumed, all L's equal)



Ideal (Desired) biasing



V_{FB} insertion



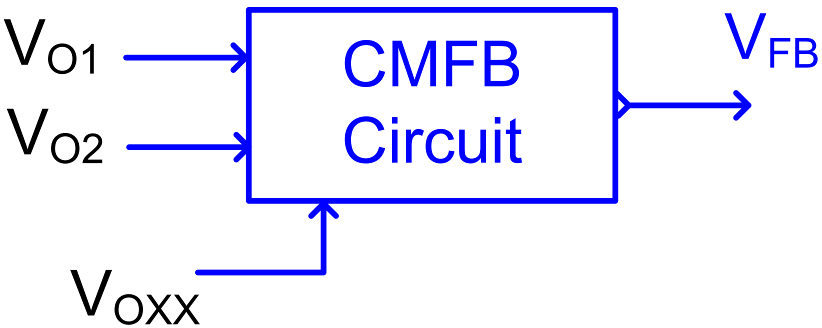
Partitioned V_{FB} insertion

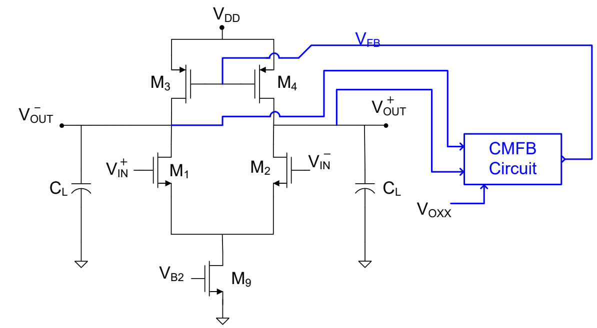
$$W_{3A} + W_{3B} = W_3$$

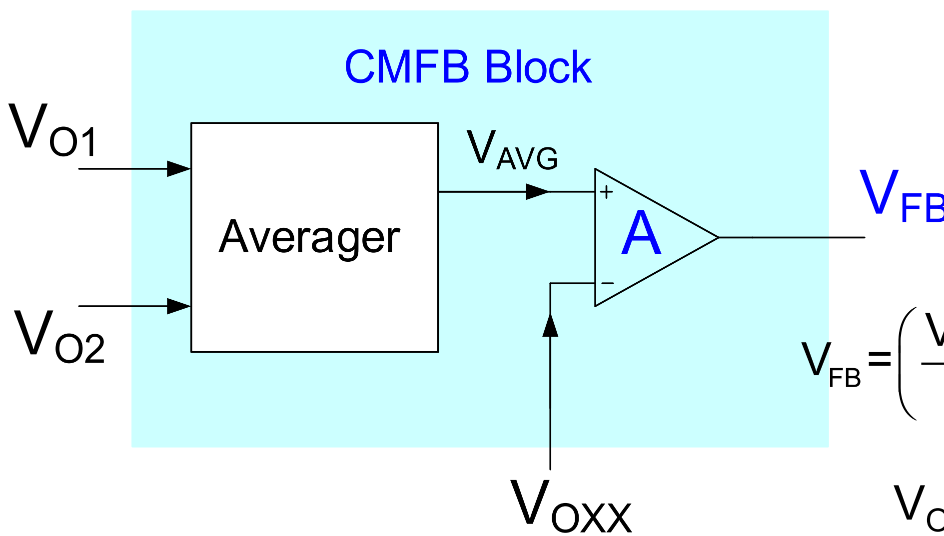
$$W_{3B} << W_{3A}$$

Of course L/R symmetry is assumed

Basic Operation of CMFB Block





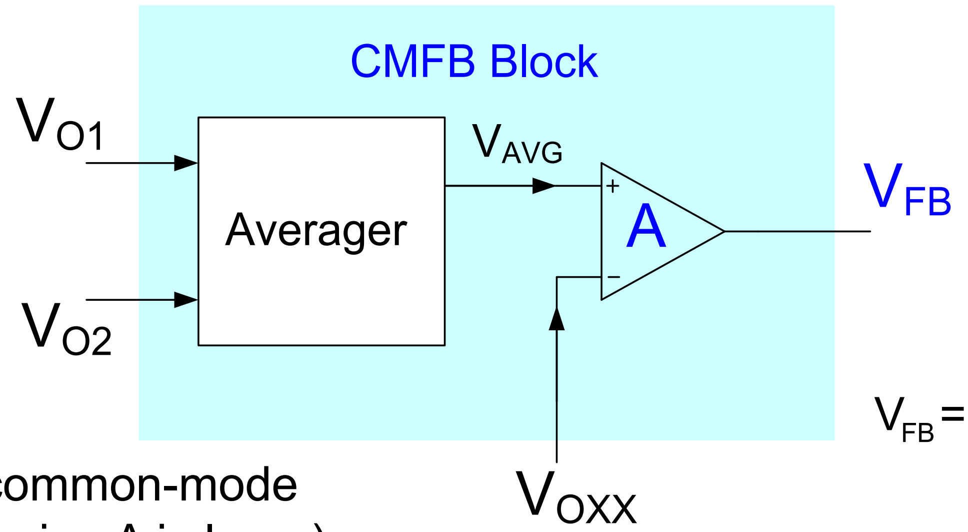


$$V_{FB}=\left(\frac{V_{01}+V_{02}}{2}-V_{OXX}\right)A(s)$$

V_{OXX} is the desired quiescent voltage at the stabilization node

(irrespective of where V_{FB} goes)

Basic Operation of CMFB Block



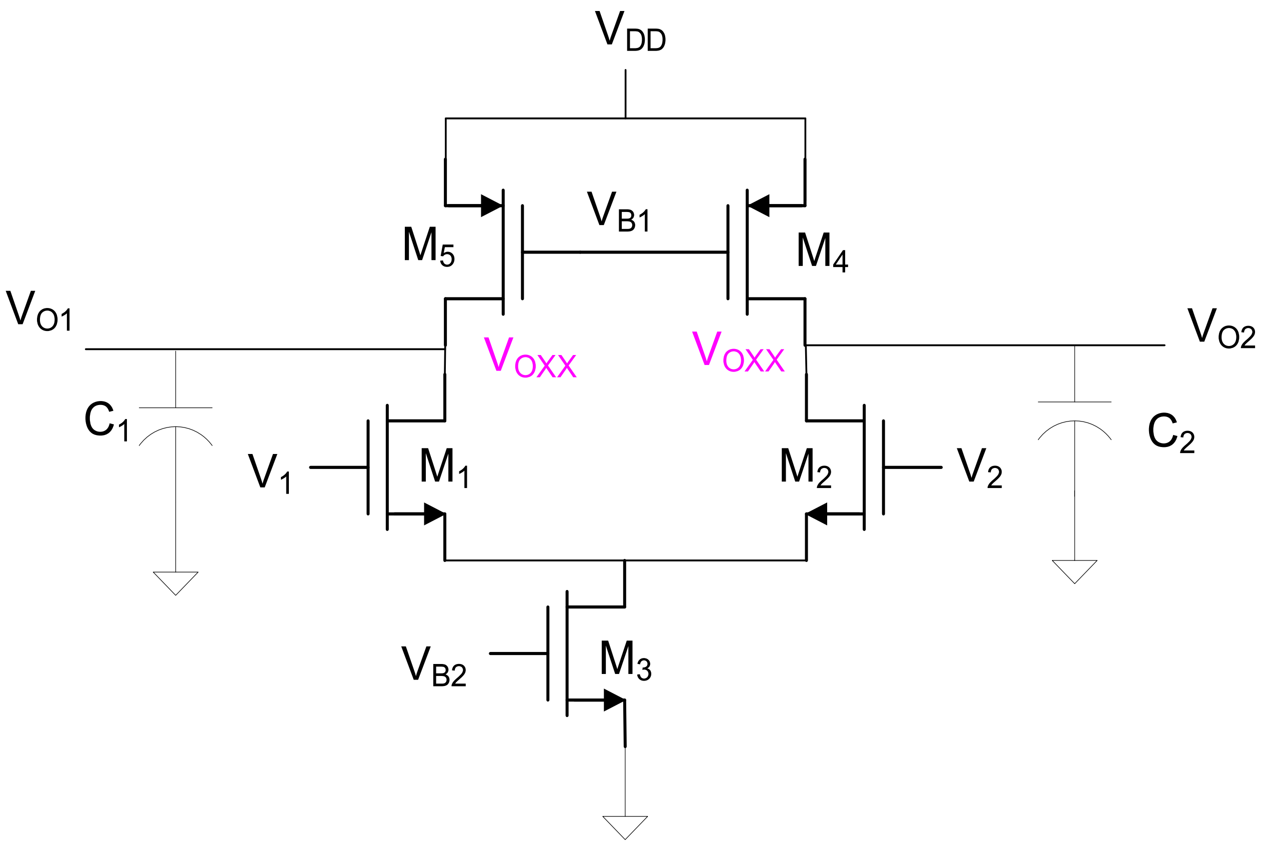
$$V_{FB} = \left(\frac{V_{01} + V_{02}}{2} - V_{OXX} \right) A(s)$$

V_{OXX} is the desired common-mode output voltage (assuming A is large)

- Comprised of two fundamental blocks
  - Averager
  - Differential amplifier
- Sometimes combined into single circuit block
- CMFB is often a two-stage amplifier so compensation of the CMFB path often required !!

Mathematics behind CMFB

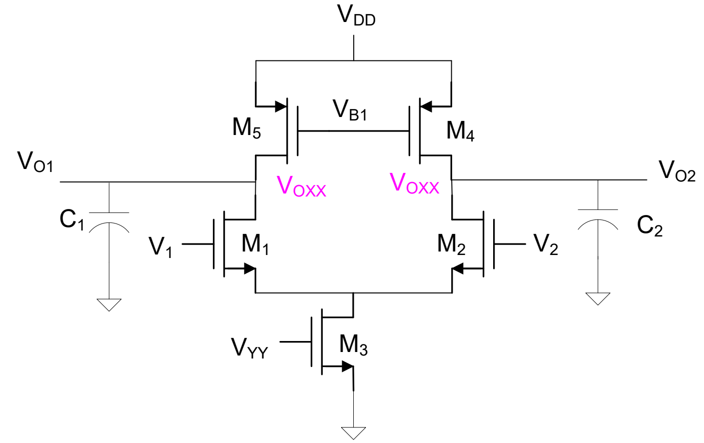
(consider an example that needs a CMFB)

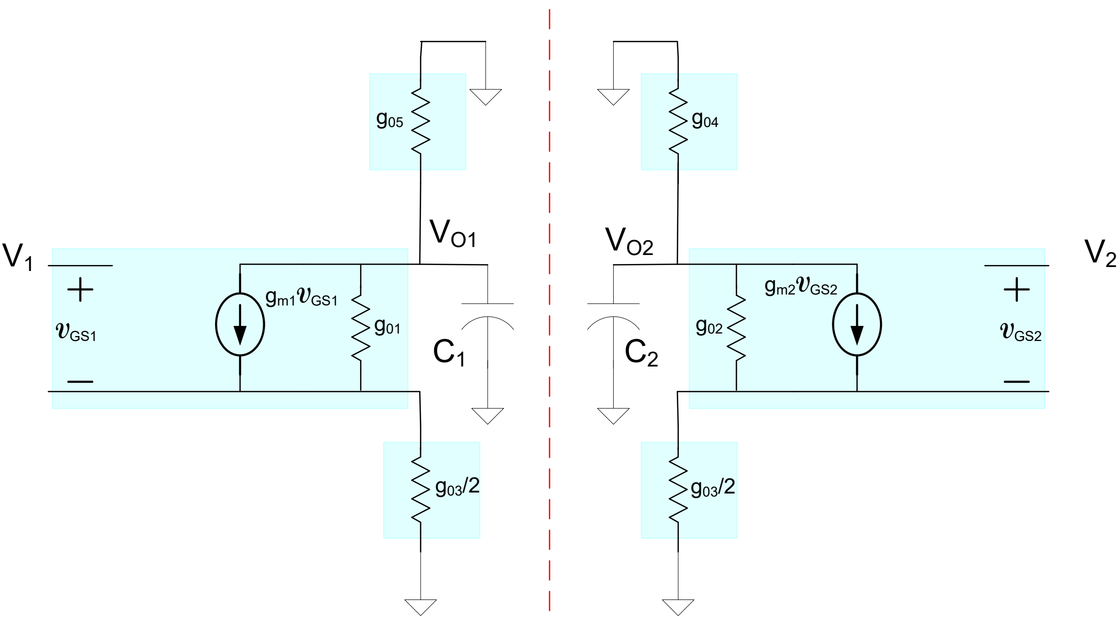


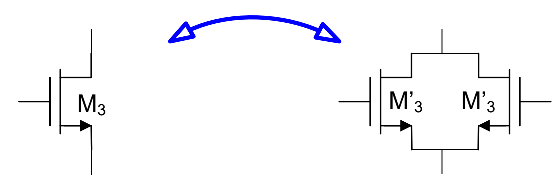
Notice there are two capacitors and thus two poles in this circuit

Mathematics behind CMFB

(consider an example that needs a CMFB)







$2W'_3=W_3$

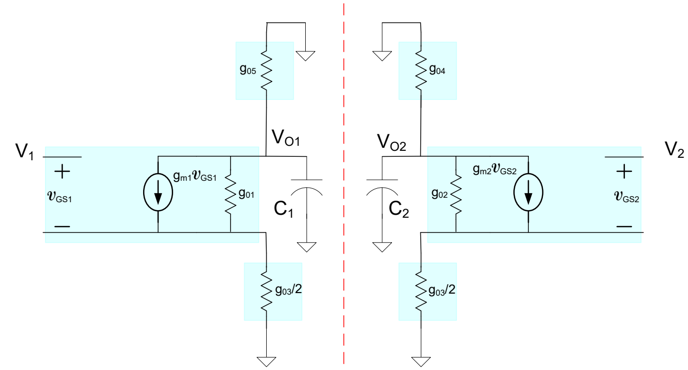
Small-signal model showing axis of symmetry (for $V_1=V_2=V_{INQ}$ i.e. $v_1=v_2=0V$)

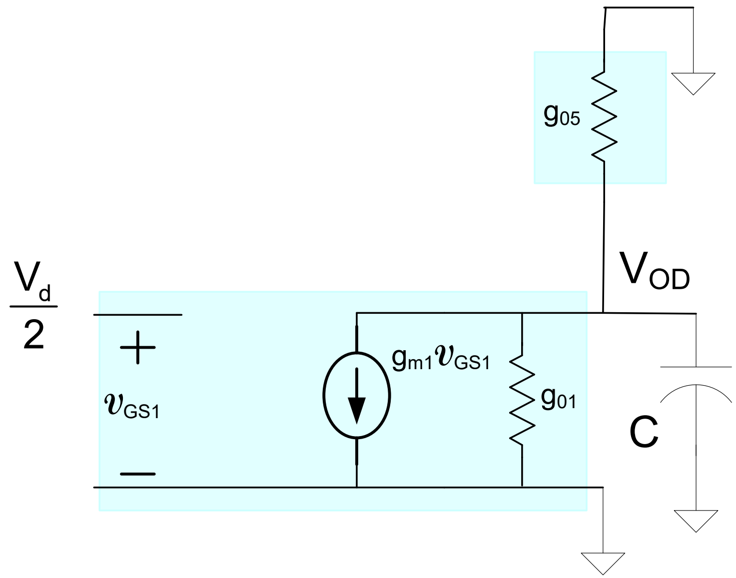
What order transfer functions are expected (note two capacitors!)?

Mathematics behind CMFB

(consider an example that needs a CMFB)

First, lets look at differential half-circuit





Small-signal difference-mode half circuit

$$V_{OD}\left(sC+g_{01}+g_{05}\right)+g_{m1}\frac{V_d}{2}=0$$

$$A_{DIFF}=\frac{-\frac{g_{m1}}{2}}{sC+g_{01}+g_{05}}$$

$$p_{DIFF}=-\frac{g_{01}+g_{05}}{C}$$

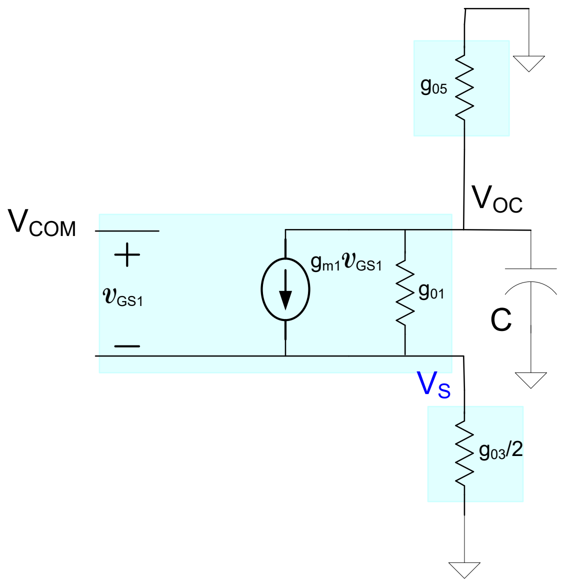
Note there is a single-pole in this circuit

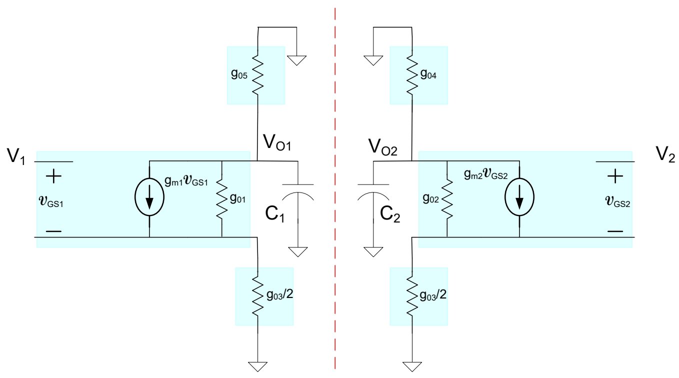
What happened to the other pole?

Mathematics behind CMFB

(consider an example that needs a CMFB)

Now lets look at common-mode half-circuit





Standard small-signal common-mode half circuit

$$V_{OC}\left(sC+g_{01}+g_{05}\right)+g_{m1}\left(V_{COM}-V_S\right)=0$$

$$V_S\left(g_{01}+g_{03}/2\right)-g_{m1}\left(V_{COM}-V_S\right)=V_{OC}g_{01}$$

$$A_{COM}=\frac{-g_{m1}\left(g_{01}+g_{03}/2\right)}{\left(sC+g_{01}+g_{05}\right)\left(g_{m1}+g_{01}+g_{03}/2\right)-g_{m1}g_{01}}\cong -\frac{g_{01}+g_{03}/2}{sC+g_{05}}$$

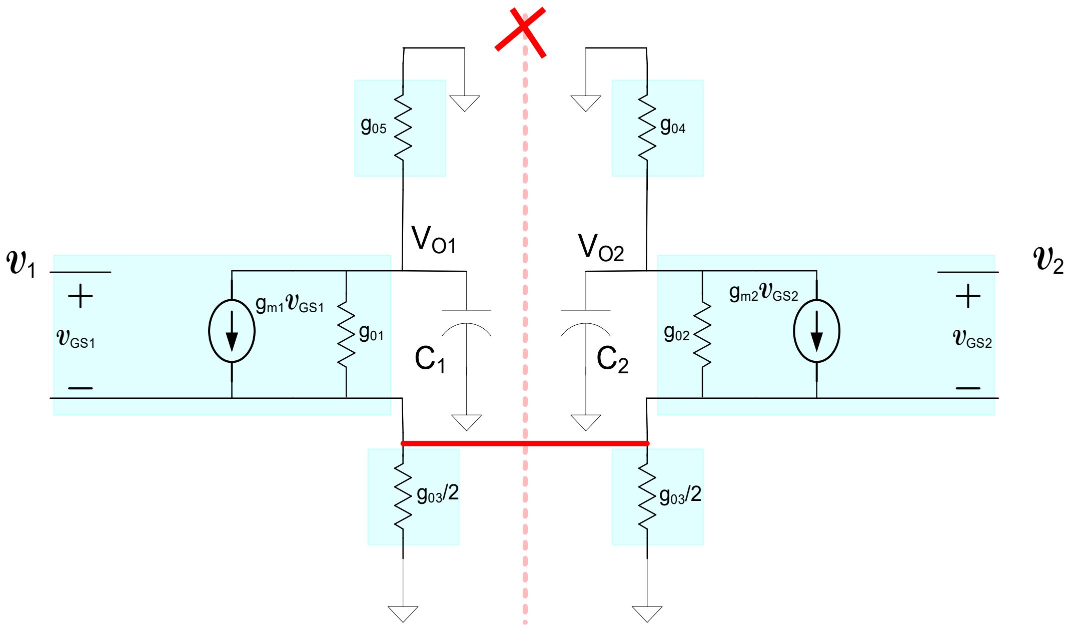
$$p_{COM}=-\frac{g_{05}}{C}$$

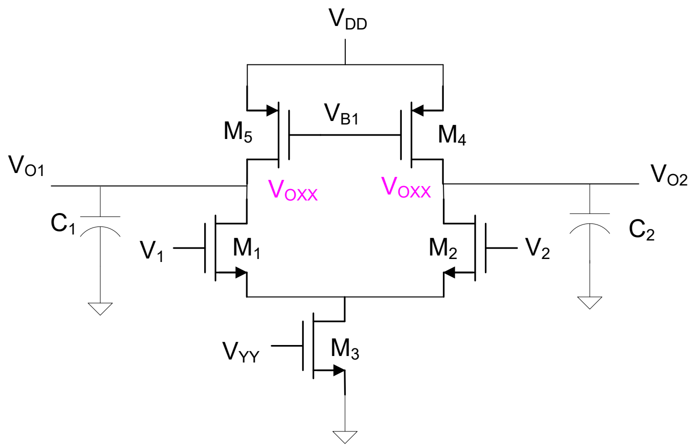
Note there is a single-pole in this circuit

And this is different from the difference-mode pole

But the common-mode gain tells little, if anything, about the CMFB

Mathematics behind CMFB





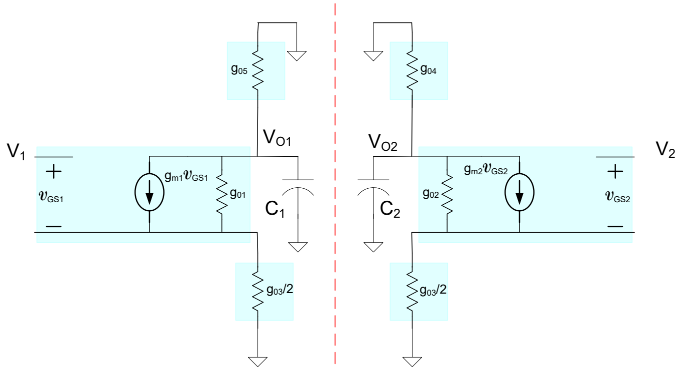
Second-order gain functions would have occurred had we not created symmetric half-circuits by assuming $v_1 = v_2$

Mathematics behind CMFB

(consider an example that needs a CMFB)

$$A_{COM} \simeq -\frac{g_{01}+g_{03}/2}{sC+g_{05}} \qquad p_{COM} = -\frac{g_{05}}{C}$$

$$A_{DIFF} = \frac{-\frac{g_{m1}}{2}}{sC+g_{01}+g_{05}} \qquad p_{DIFF} = -\frac{g_{01}+g_{05}}{C}$$



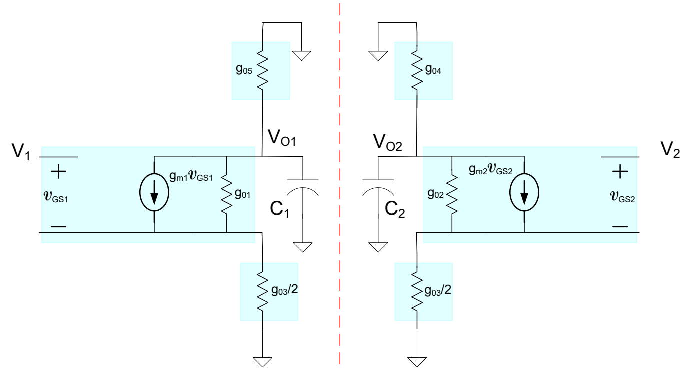
- Difference-mode analysis of symmetric circuit completely hides all information about common-mode
- This also happens in simulations
- Common-mode analysis of symmetric circuit completely hides all information about difference-mode
- This also happens in simulations
- Difference-mode poles may move into RHP (for two-stage structures) with FB so compensation is required for proper operation (or stabilization)
- Common-mode poles may move into RHP (for two-stage structures) with FB so compensation is required for proper operation (or stabilization)
- Difference-mode simulations tell nothing about compensation requirements for common-mode feedback
- Common-mode simulations tell nothing about compensation requirements for difference-mode feedback

Mathematics behind CMFB

(consider an example that needs a CMFB)

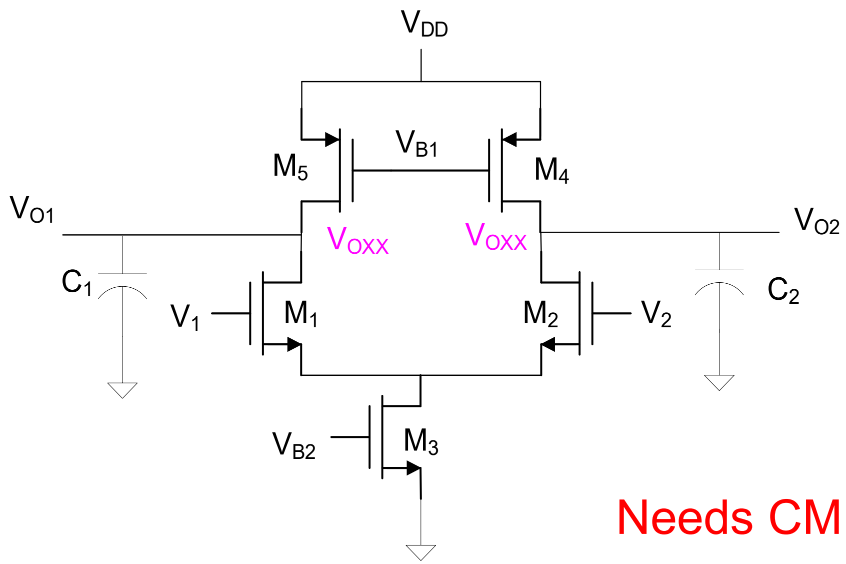
$$A_{COM} \simeq -\frac{g_{01}+g_{03}/2}{sC+g_{05}} \qquad p_{COM} = -\frac{g_{05}}{C}$$

$$A_{DIFF} = \frac{-\frac{g_{m1}}{2}}{sC+g_{01}+g_{05}} \qquad p_{DIFF} = -\frac{g_{01}+g_{05}}{C}$$



- Common-mode and difference-mode gain expressions often include same components though some may be completely absent in one or the other mode
- Compensation capacitors can be large for compensating either the common-mode or difference-mode circuits
- Highly desirable to have the same compensation capacitor serve as the compensation capacitor for both difference-mode and common-mode operation
  - But tradeoffs may need to be made in phase margin for both modes if this is done
- Better understanding of common-mode feedback is needed to provide good solutions to the problem

Does this amplifier need compensation?



Needs CMFB

No – because it is a single-stage amplifier ?

The difference-mode circuit of this 5T op amp usually does not need compensation ?

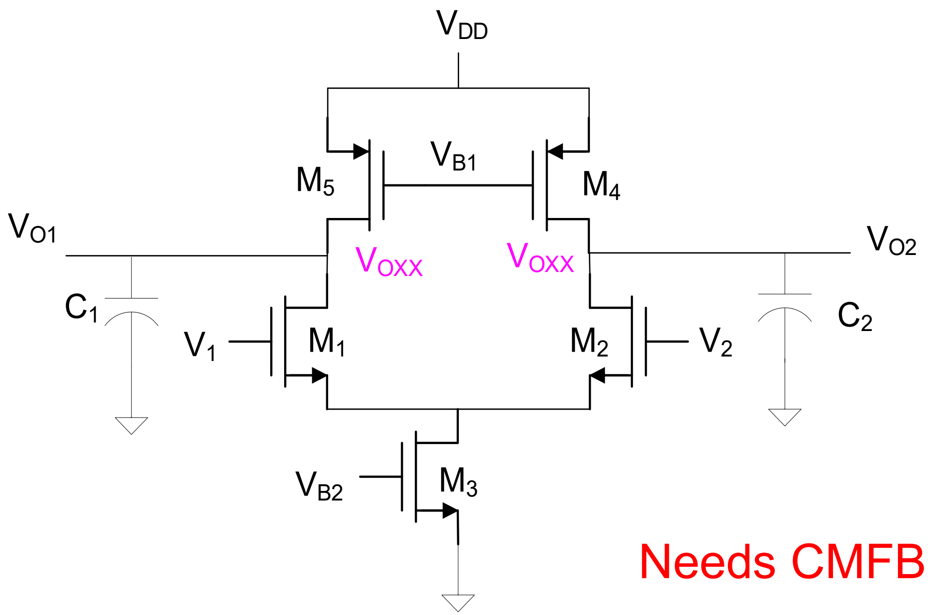
But what about the common-mode operation?

No – because the common-mode circuit is also a single-stage circuit?

What are the common-mode inputs for CMFB? **V_{B1} or V_{B2}**

But observe that the common-mode inputs V_{1C} and V_{2C} are not the common-mode inputs for the CMFB?

Does this amplifier need compensation?



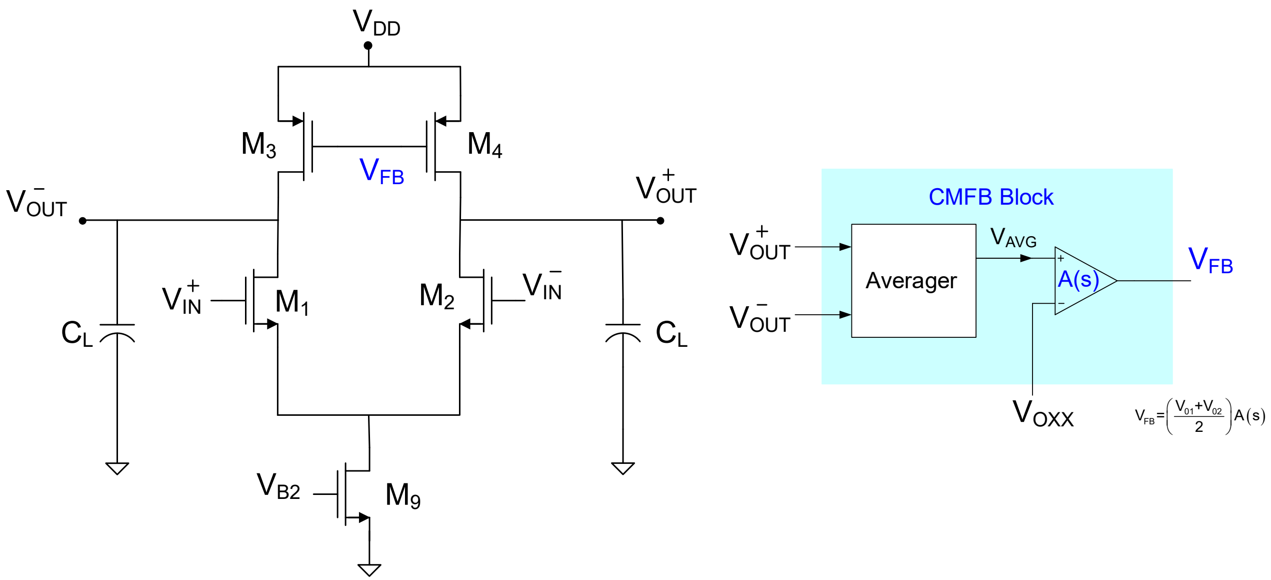
This circuit has 3 different natural common-mode inputs:

$$V_{B1},\ V_{B2},\ \frac{V_1+V_2}{2}$$

V_{B1} or V_{B2} (or possibly both in some way) are the inputs for CMFB

Can it be argued that it is still a single-stage common-mode circuit irrespective of which common-mode input is used and thus compensation of the common-mode circuit will not be required?

Does this amplifier need compensation?



The CMFB path from V_{FB} back to V_{FB} is a two-stage feedback amplifier comprised of the common-mode gain of the basic 5T circuit from V_{FB} to V_{OUT} and the common-mode gain from V_{OUT} to V_{FB}

This amplifier needs compensation (of the CMFB path) even if the basic amplifier is single-stage

The overall amplifier including the β amplifier for the differential feedback path should be considered when compensating the CMFB circuit

If a second-stage is added to the 5T op amp, the compensation network for the differential stage <u>may</u> also provide the needed compensation for the CMFB path

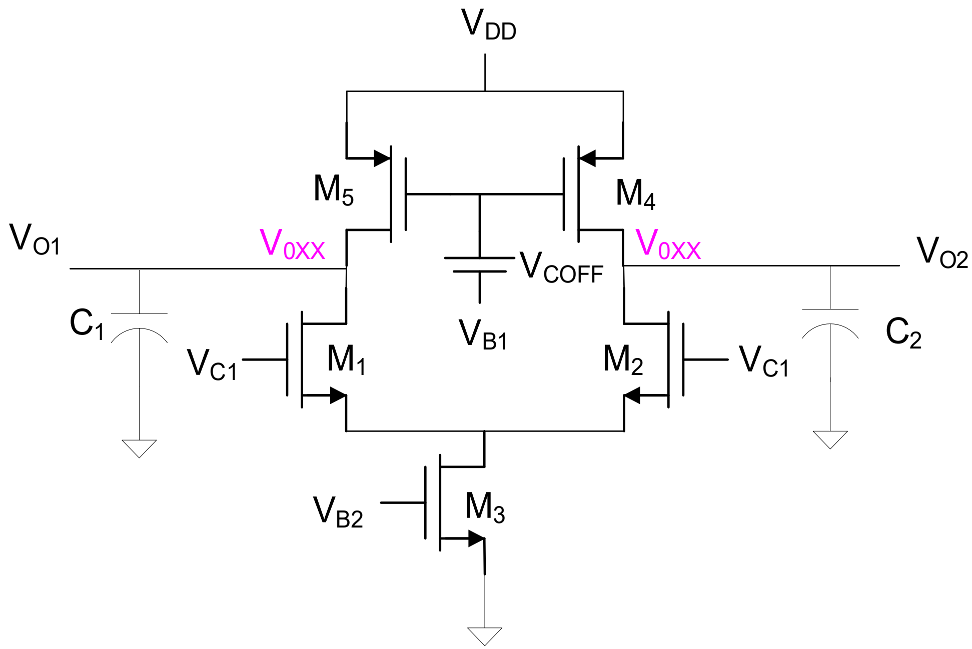
Common-Mode and Difference-Mode Issues

Overall poles are the union of the common-mode and difference mode poles

Separate analysis generally required to determine common-mode and difference-mode performance

Some amplifiers will need more than one CMFB

Common-mode offset voltage



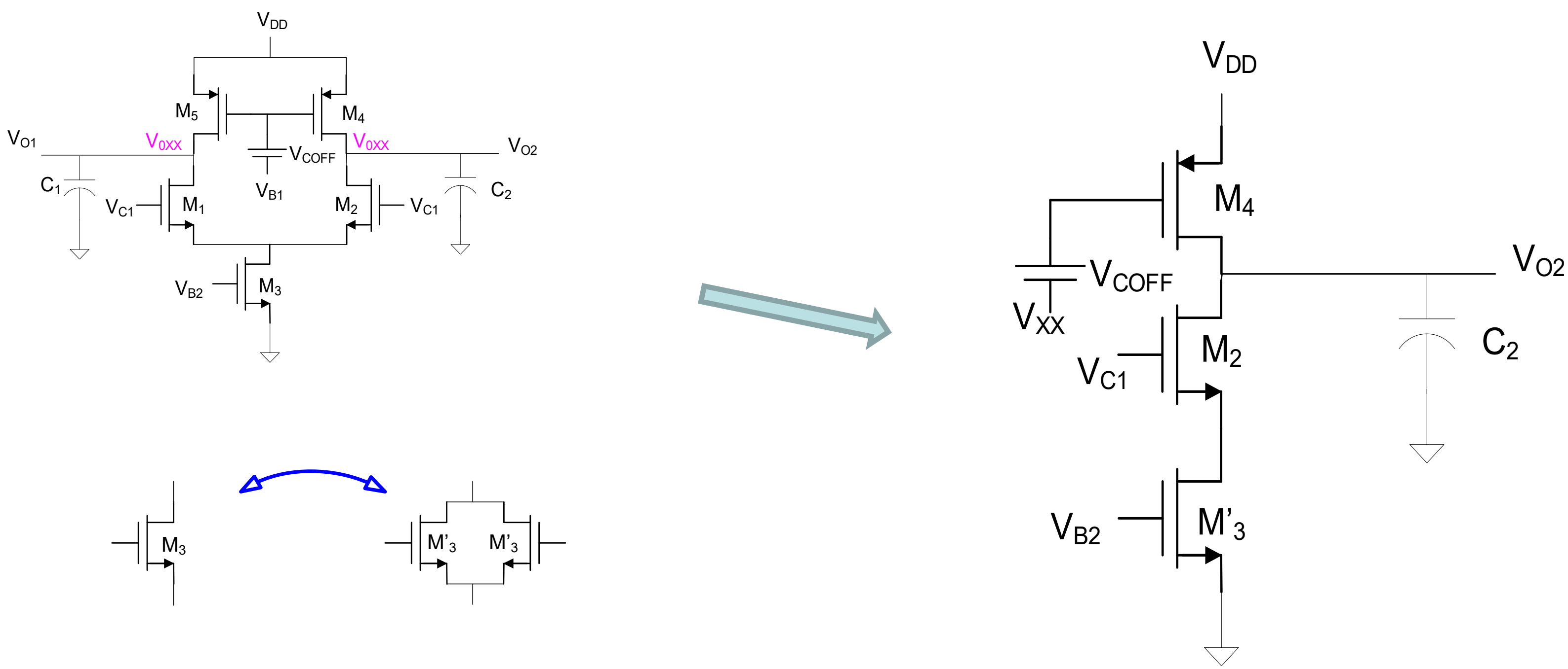
Assume ideally V_{B1} will provide the desired value for V_{OXX}

Definition: The common-mode offset voltage is the branch voltage that must be applied to the biasing node at the CMFB point to obtain the desired operating point at the stabilization node

Note: Could alternately define common-mode offset relative to V_{B2} input if CMFB to M_3

Common-mode offset voltage

Consider again the Common-mode half circuit



There are three common-mode inputs to this circuit !

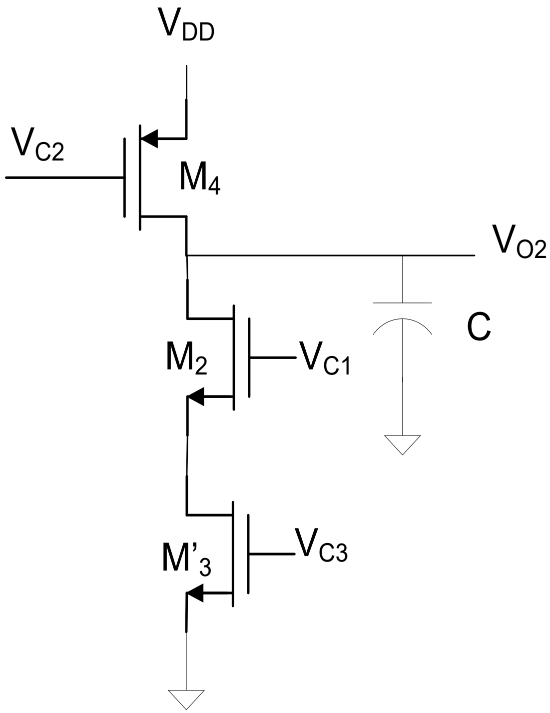
The common-mode signal input is distinct from the input that is affected by V_{COFF}

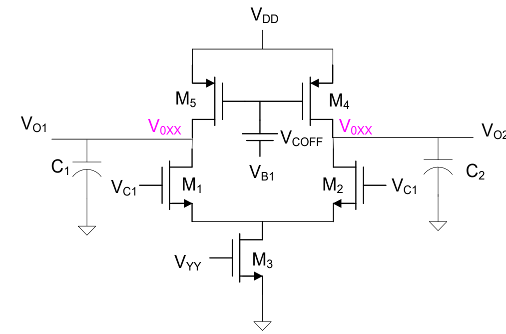
The gain from the common-mode input where V_{FB} is applied may be critical !

How do the poles from the three different CM inputs relate to each other?

They are the same!!

Common-mode gains





$$A_{COM0} \cong -\frac{g_{02}+g_{03}/2}{g_{04}} = -\frac{\lambda I_T}{\lambda I_T/2} = -\frac{1}{2}$$

$$A_{COM20} \cong -\frac{g_{m4}}{g_{04}} = -\frac{2I_T/V_{EB4}}{\lambda I_T/2} = -\frac{4}{V_{EB4}\lambda}$$

$$A_{COM30} \cong -\frac{g_{m3}/2}{g_{04}} = -\frac{\frac{2I_T}{V_{EB3}}/2}{\lambda I_T/2} = -\frac{2}{\lambda V_{EB3}}$$

$$A_{COM} = \frac{V_{02}}{V_{C1}} \cong -\frac{g_{02}+g_{03}/2}{sC+g_{04}}$$

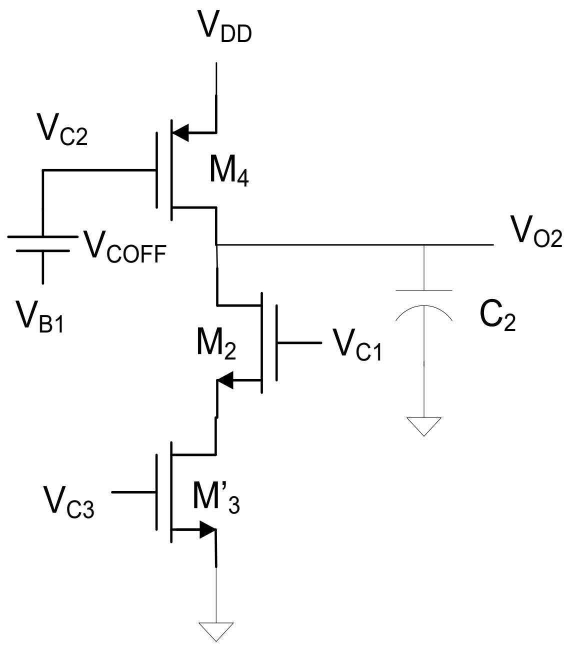
$$A_{COM2} = \frac{V_{02}}{V_{C2}} \cong -\frac{g_{m4}}{sC+g_{04}}$$

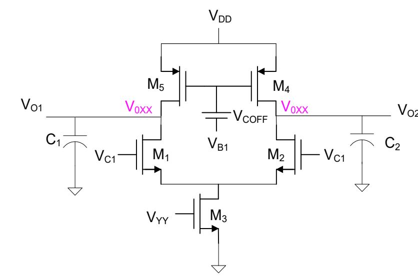
$$A_{COM3} = \frac{V_{02}}{V_{C3}} \cong -\frac{g_{m3}/2}{sC+g_{04}}$$

Although the common-mode gain A_{COM0} is very small, A_{COM20} is very large! (but can be reduced by partitioning M_4)

Shift in V_{02Q} from V_{OXX} is the product of the common-mode offset voltage and A_{COM20}

Effect of common-mode offset voltage





$$A_{COM20} \cong -\frac{4}{V_{EB5}\lambda}$$

$$\Delta V_{02} = A_{COM20} V_{COFF}$$

How much change in V_{02} is acceptable? (assume e.g. 50mV)

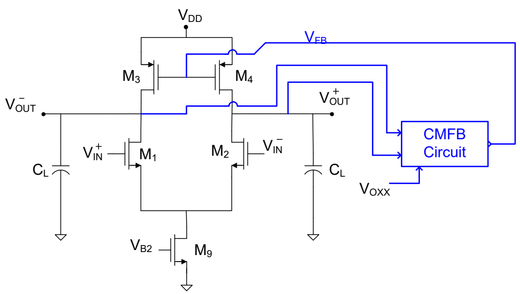
How big is V_{COFF}? (similar random expressions for V_{OS}, assume, e.g. 25mV) (that due to process variations even larger)

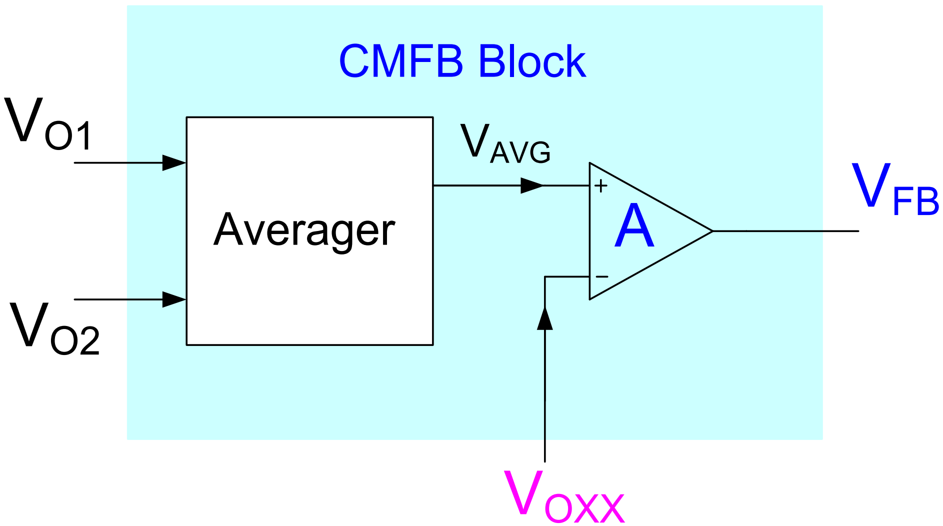
How big is A_{COM20}? (if λ=.01, V_{EB}=.2, A_{COM20}=2000)

If change in V_{02} is too large (and it usually is), a CMFB circuit is needed

(50mV >? 2000x25mV)

How much gain is needed in the CMFB amplifier?



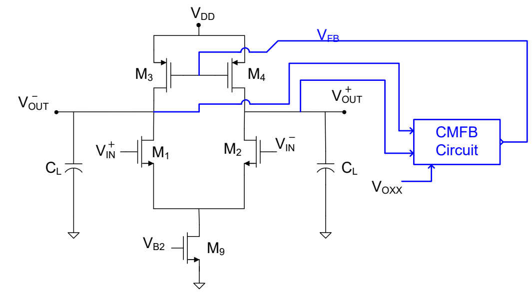


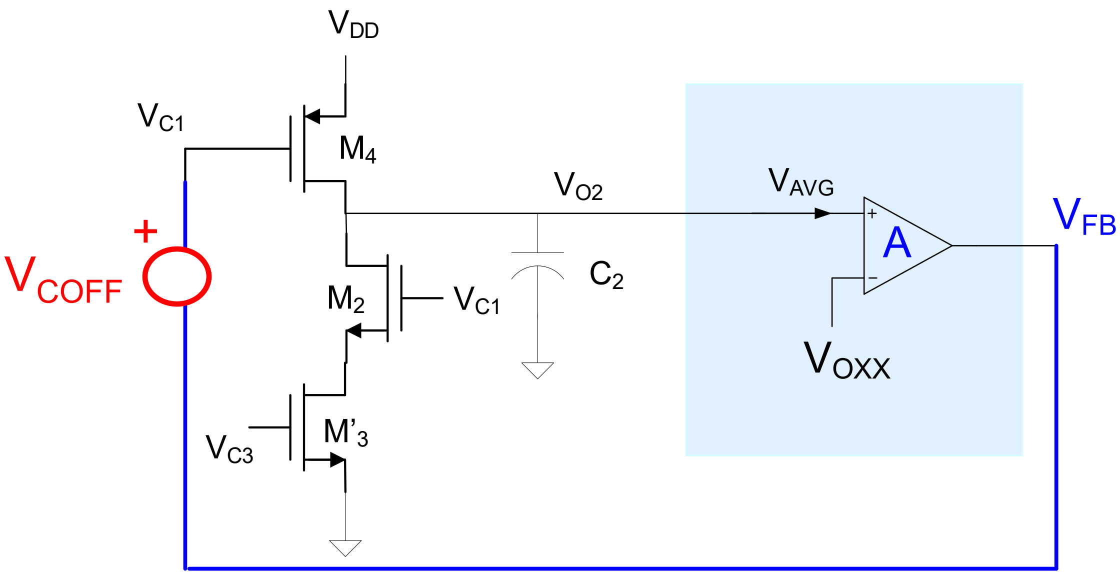
CMFB must compensate for V_{COFF}

Want to guarantee $\left|V_{02Q}-V_{0XX}\right| < \Delta V_{OUT\text{-}ACCEPTABLE}$

This is essentially the small-signal output with a small-signal input of V_{COFF}

How much gain is needed in the CMFB amplifier?





The CMFB Loop

Want to guarantee

$$\left|V_{02Q}-V_{0XX}\right| < \Delta V_{OUT\text{-}ACCEPTABLE}$$

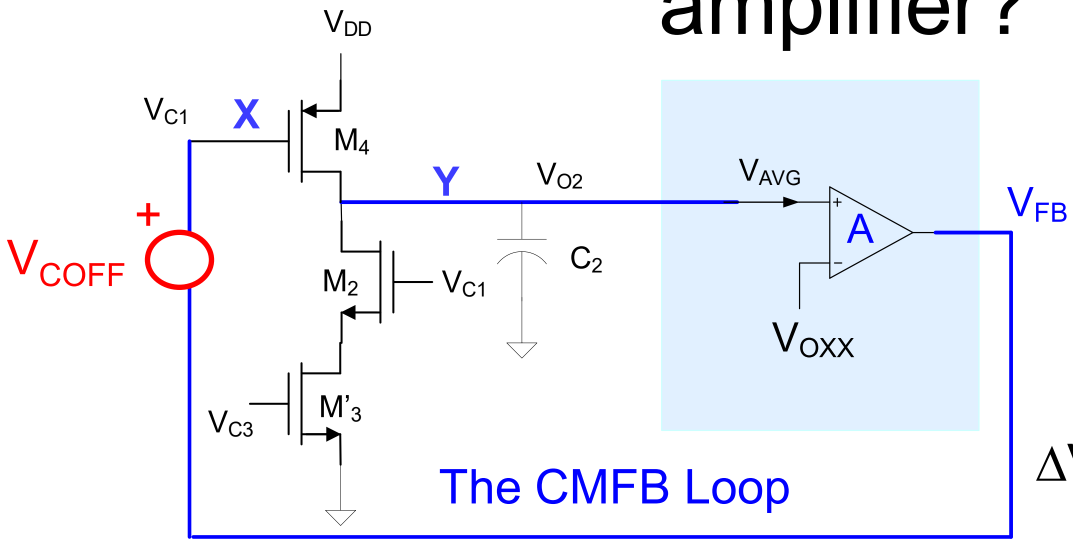
Consider the small-signal part of V_{02} (notation not shown below) and do a small-signal analysis, only input is V_{COFF}

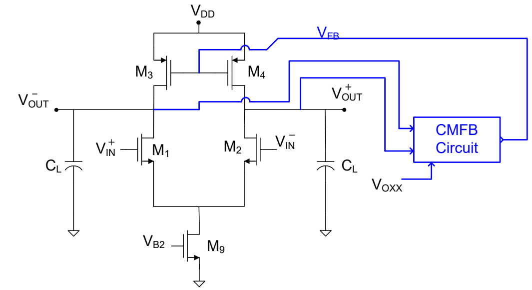
$$V_{02}=\left(V_{02}A+V_{COFF}\right)A_{COM2}$$

$$V_{02}=V_{COFF}\frac{A_{COM2}}{1-AA_{COM2}}$$

$$\Delta V_{0UT\text{-}ACCEPTABLE}=V_{COFF}\frac{A_{COM2}}{1-AA_{COM2}}$$

How much gain is needed in the CMFB amplifier?





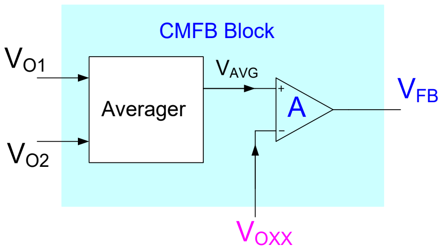
$$\Delta V_{0UT\text{-}ACCEPTABLE} = V_{COFF}\frac{A_{COM2}}{1-AA_{COM2}}$$

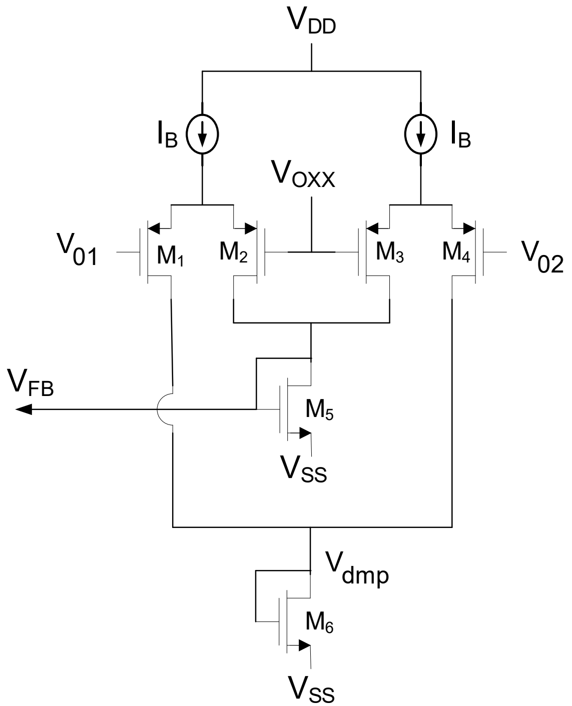
- Node **Y** is common to both differential feedback loop and CMFB loop
- This does not require a particularly large gain
- This is the loop that must be compensated since A and A_{COMP2} will be frequency dependent
- Miller compensation capacitor for compensation of differential loop will often appear in shunt with C_2
- Can create this "half-circuit" loop (without CM inputs on a fully differential structure) for simulations
- Results extend readily to two-stage structures with no big surprises
- Capacitances on nodes **X** and **Y** as well as compensation C in A amplifier (often same as capacitor on **Y** node) create poles for CMFB circuit
- Reasonably high closed-loop CMFB bandwidth needed to minimize shifts in output due to high-frequency common-mode noise

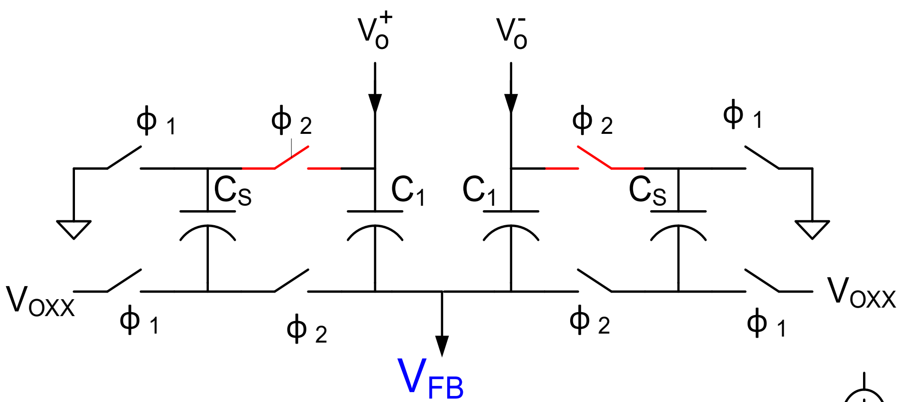
Compensation of CMFB loop will affect differential compensation if C_2 needs to be changed

CMFB Circuits

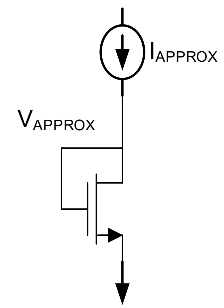
- Several (but not too many) CMFB blocks are widely used
- Can be classified as either continuous-time or discrete-time





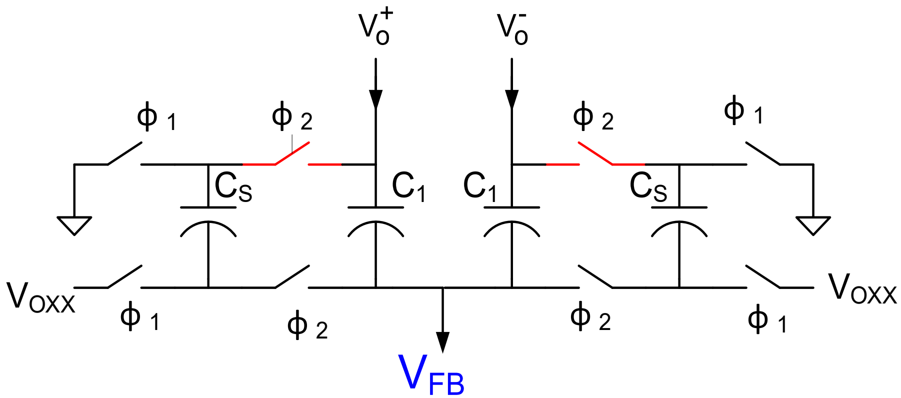


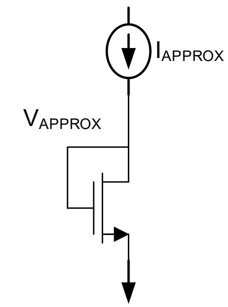
C_S small compared to C_1



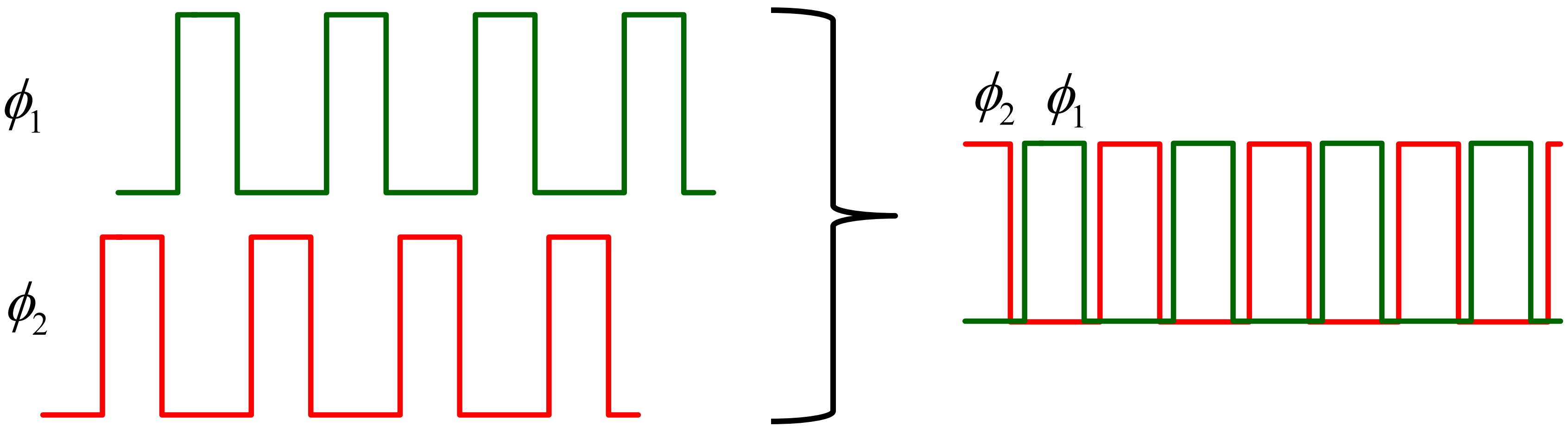
- V_{OXX} generated by simple bias generator
- φ_1 and φ_2 are complimentary non-overlapping clocks that run continuously
- At this point, think of V_{dmp} as a place to “dump” the current from the diff pairs
- But V_{dmp} does contain the same information as V_{FB}, only of opposite sign!

CMFB Circuits





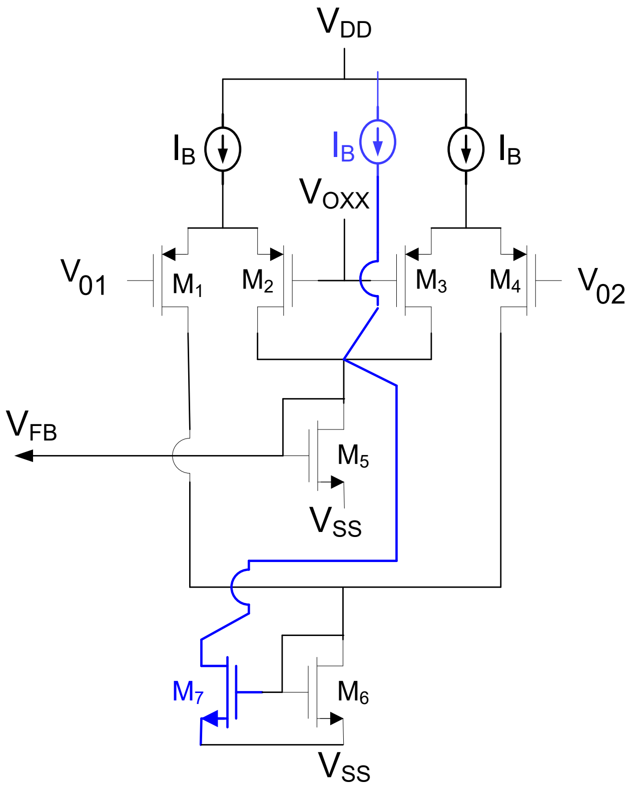
φ_1 and φ_2 are complimentary non-overlapping clocks that run continuously

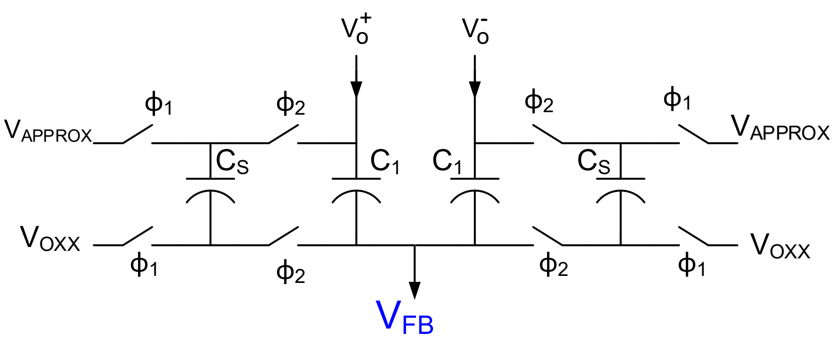


- non-overlap of φ_1 and φ_2 is critical but frequency is not critical
- Could even have 25% or less duty cycle to guarantee non-overlap
- φ_1 and φ_2 run asynchronously with respect to the op amp

CMFB Circuits

Several (but not too many) CMFB circuits exist
Can be classified as either continuous-time or discrete-time

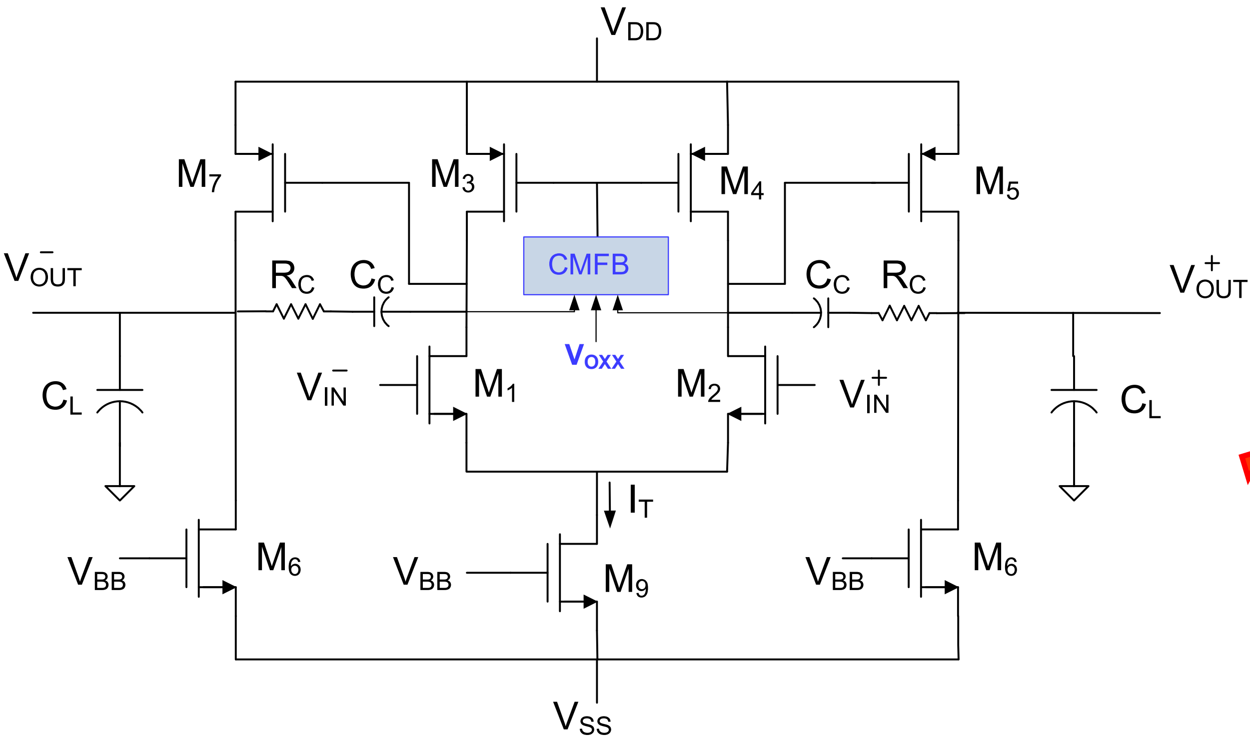


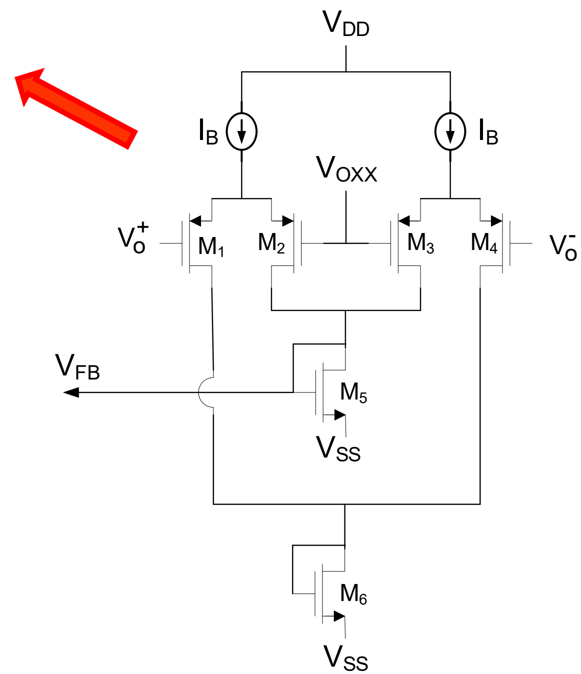


Circuit in blue can be added to double CMFB gain

CMFB Circuits

Fully-Differential two-stage Op Amp with CMFB





Output Stages

All op amps discussed so far are actually transconductance amplifiers with high (and often very high) output impedance

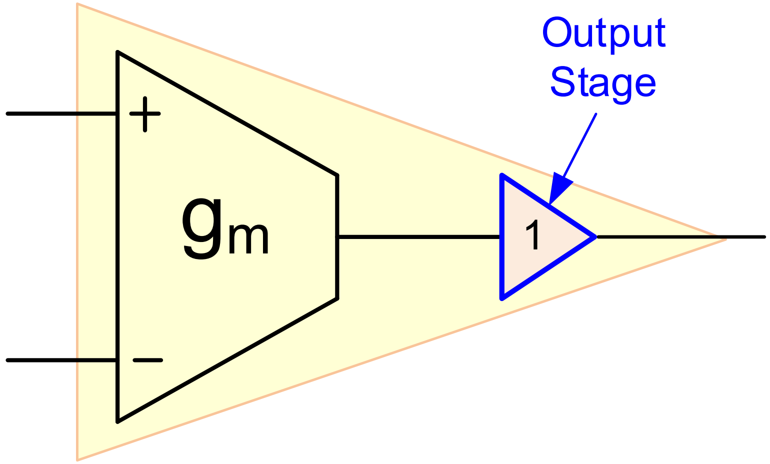
If resistive feedback is applied, loading by the β network will invariably dramatically drop the effective open-loop op amp gain (maybe 40dB to 80dB drop) thereby rendering the op amp nearly useless !

Output stages are often added to reduce (or often eliminate) this drop in gain

Output stage not needed if all loading is capacitive

Output Stages

The Concept:



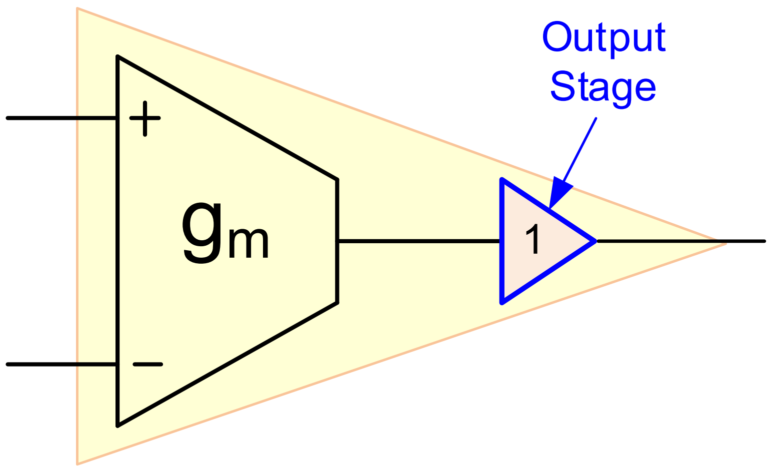
Output stage should have infinite input impedance and low output impedance

Increases the number of stages by 1 but want frequency response to not be affected by output stage

Frequency response of output stage should be high so it does not introduce additional poles that interfere with compensation of the high impedance amplifier

Output Stages

The Concept:



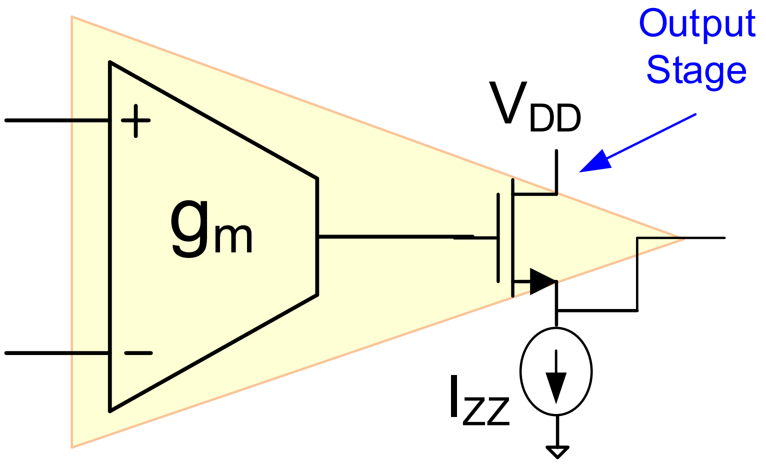
Output stage should have infinite input impedance and low output impedance

Increases the number of stages by 1 but want frequency response to not be affected by output stage

Frequency response of output stage should be high so it does not introduce additional poles that interfere with compensation of the high impedance amplifier

Output Stages

The Concept:



Common Drain Amplifier Provides a Good Output Stage

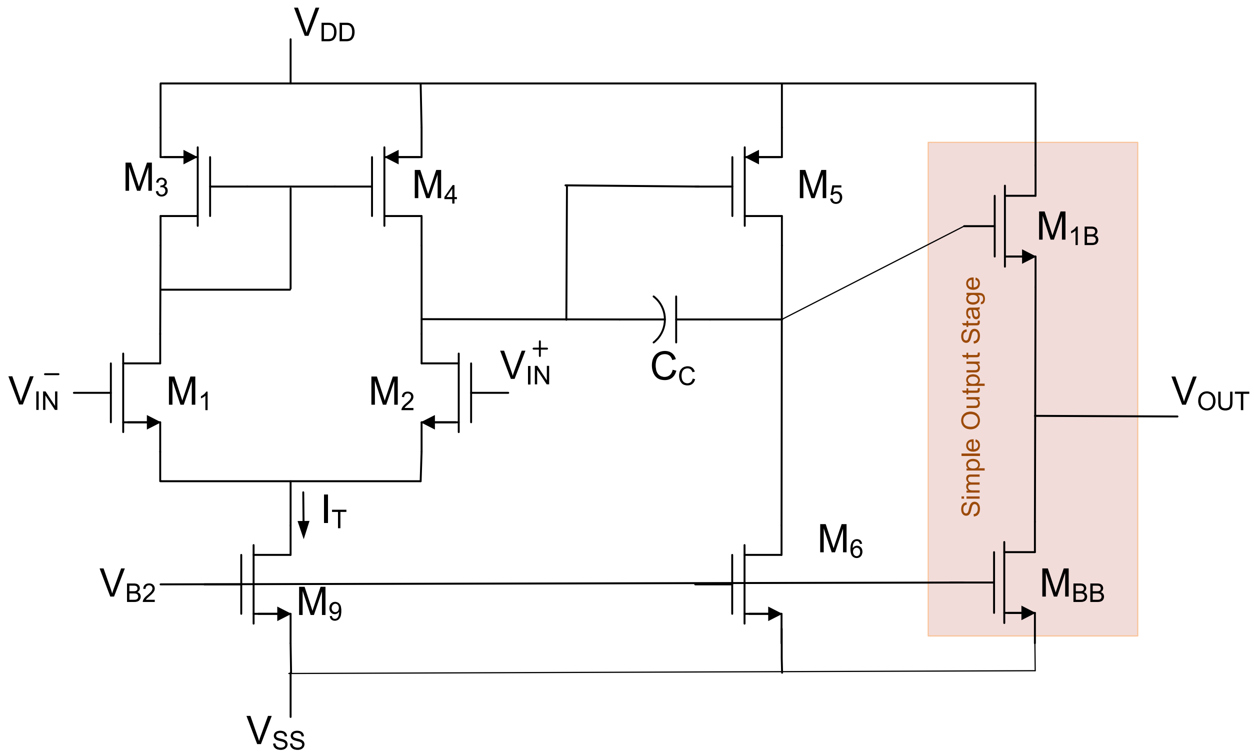
Simple structure

Some loss of output signal swing

Significant power overhead

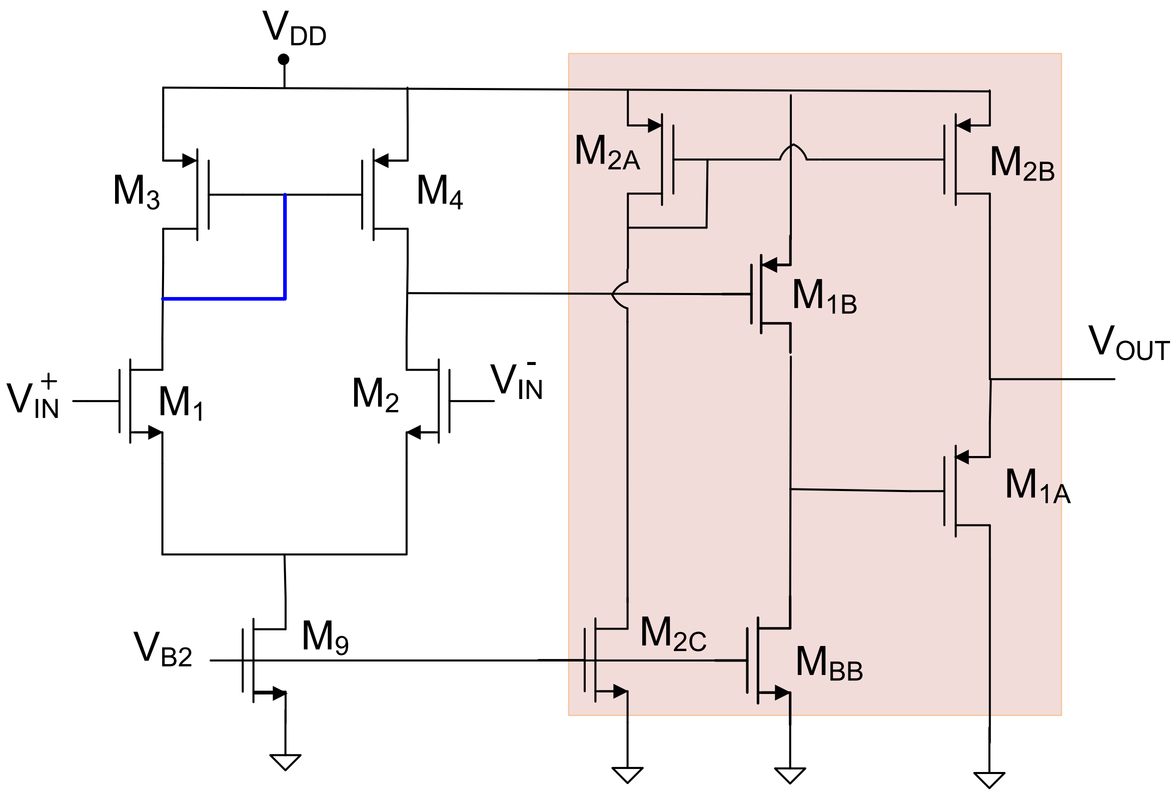
Output Stages

7T Op Amp with Simple Output Stage

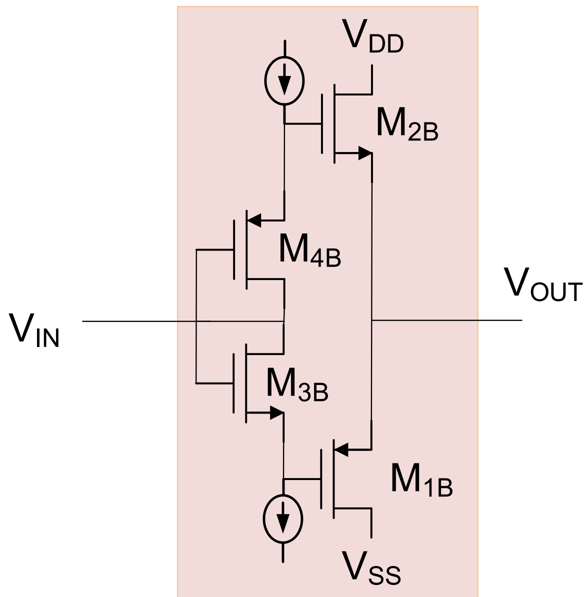


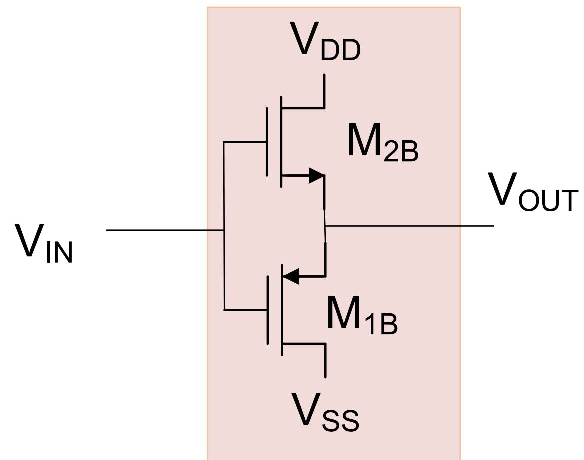
Output Stages

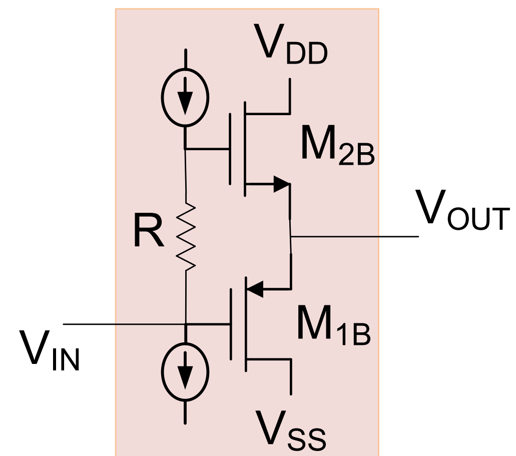
5T Op Amp with Simple Output Stage



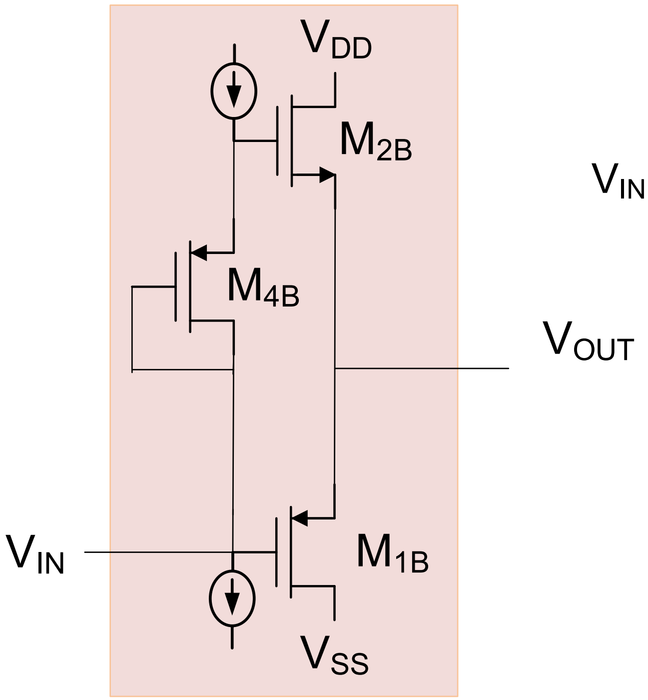
Other Selected Output Stages

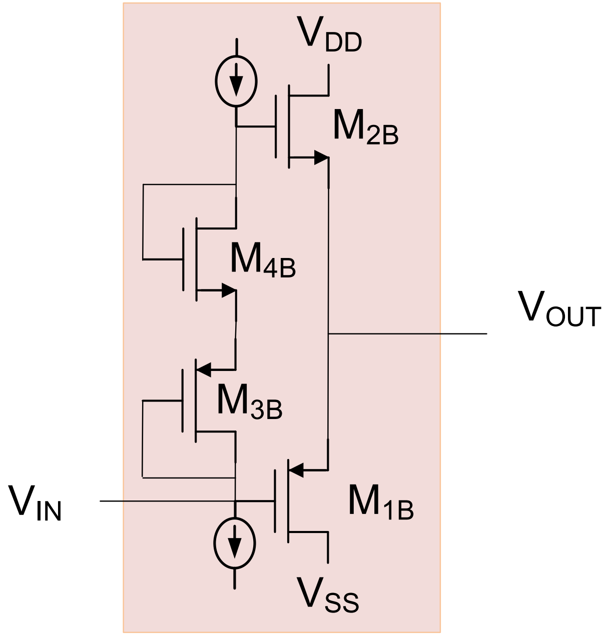


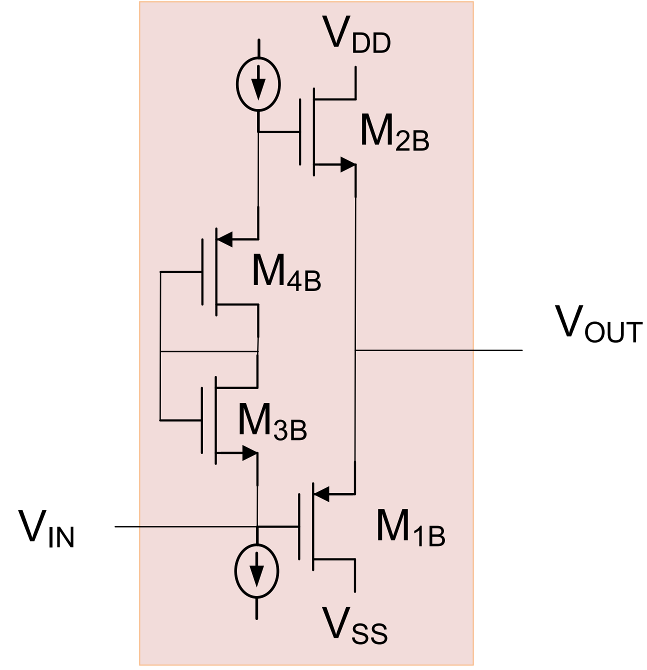




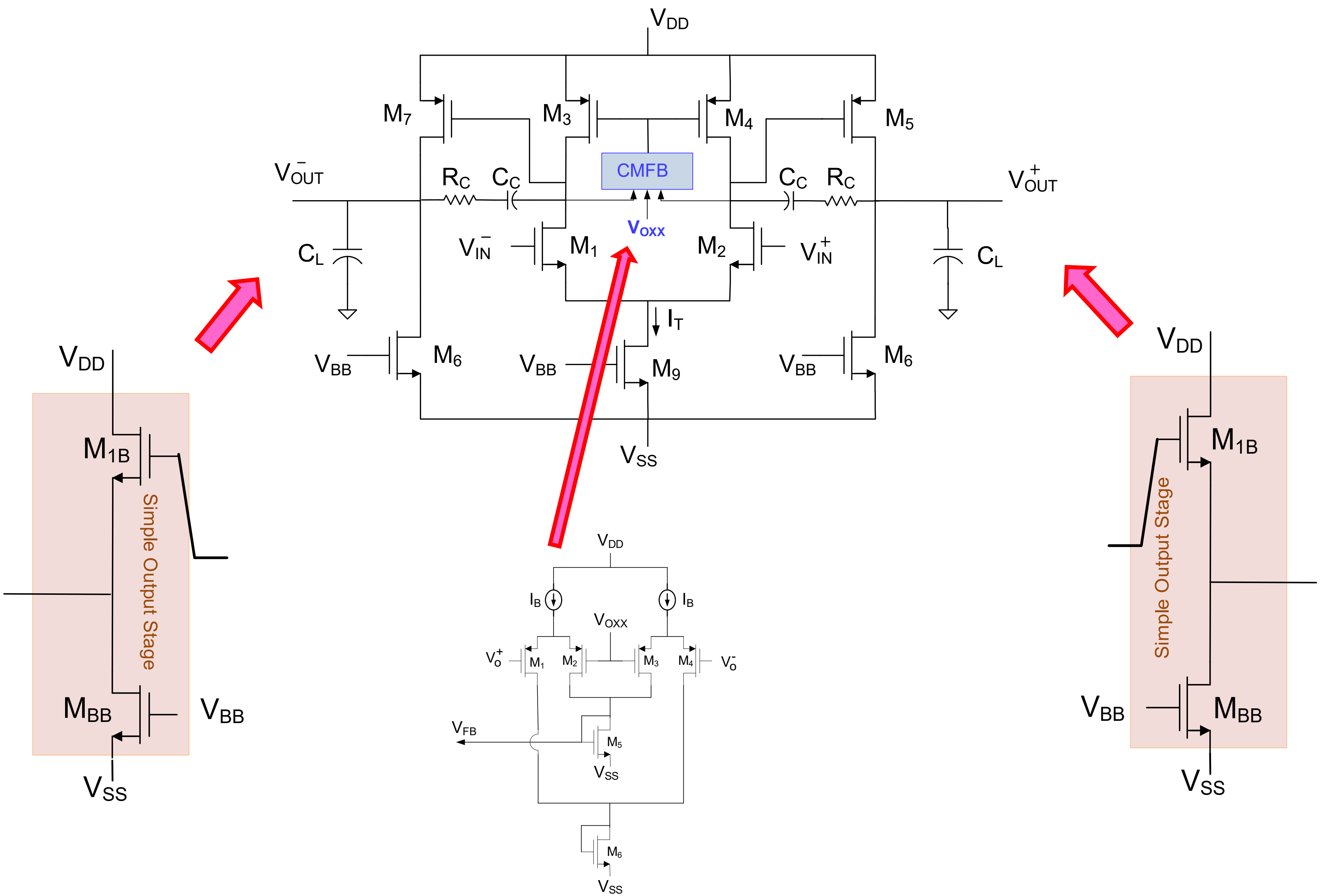
Other Selected Output Stages







Fully-Differential Op Amp with CMFB and Output Stages



Stay Safe and Stay Healthy !

End of Lecture 24